F-15 RADAR SET

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1.0 INTRODUCTION

This document presents a description of the built-in-test (BIT) capabilities of the F-15 radar set. F-15 BIT is designed to detect a radar system fault, and to isolate that fault to one of eight[1] line replaceable units (LRU) in the radar set. Further isolation within an LRU is left to other radar maintenance devices.

Figure 1-1 below illustrates the F-15 radar set block diagram. The LRU's which are tested by BIT as described herein are shown in crosshatch.

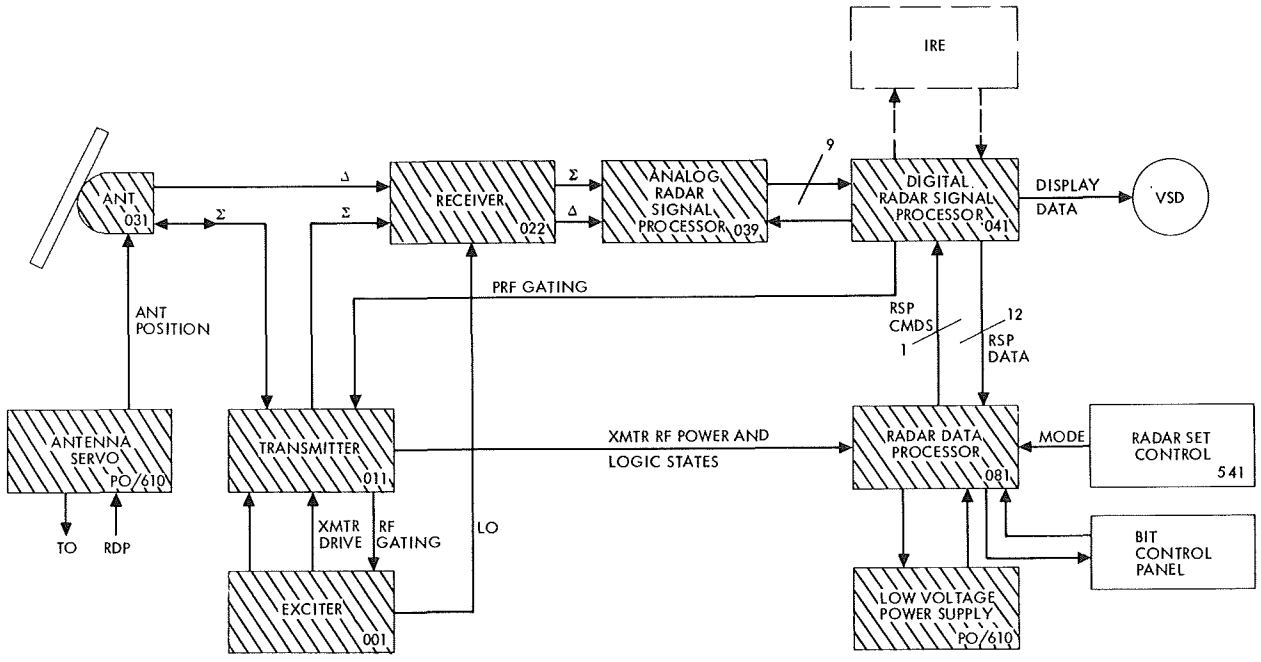

Figure 1-1. F-15 radar set.

[1] There are nine LRU's which comprise the radar set, but BIT has no test which will result in a fault isolation to the radar set control (541) unit.

To accomplish the fault detection and isolation task BIT employs both hardware and software. The BIT software, consisting of about 4000 words, resides in the radar data processor (081) unit. The function of the BIT software is scheduling of the tests, configuring the radar system for tests, and evaluation of test results. The BIT hardware provides the various test circuits and signals which are controlled by the software.

BIT test failures are recorded in a BIT matrix. The BIT matrix is described in Section 2.0. Section 2.0 consists of a series of articles which describe the various BIT tests. As much as possible, the articles have been written as stand-alone items. This has been done so that if a BIT user is interested in the details of only one test, he can read the one article relevant to the one test, without having to read the entire document. It is envisioned that a typical user would observe a radar fault, and upon reading the BIT matrix would determine which test failed. If he wished to learn some details about that test, he could turn to the relevant portion of Section 2.0.

While not intended as a teaching tool, it is hoped that this document could also provide new BIT users with a comprehensive introduction to BIT.

Section 3.0 presents a description of BIT track test. This is a qualitative test of radar performance.

Section 4.0 presents a synopsis of BIT timing. This section indicates when BIT tests are done in the various BIT modes, and how and when they are interleaved with the various tactical modes.

Section 5.0 presents a description of the hardware required to accomplish the BIT fault detection and isolation task.

The descriptions presented in this document were prepared assuming a specific combination of hardware and software. The assumptions are,

- Hardware – 081 unit with 24K memory
  022 unit with paramp
- Software – 24K Tactical program.

While most of the BIT tests are unaffected by different hardware and software changes, the mix of tests, and the scheduling of tests may change with system configuration. The changeable nature of BIT occurs as a result of hardware configuration changes; new circuits are added or deleted, and new tests must be devised to accommodate these changes.

1.1 TEST LIMITATIONS

Bit tests are designed to exercise and analyze the radar set as it normally would be used. It is therefore assumed that the radar set is configured in a normal system interconnection. Any deviation from the normal system interconnection or configuration will obviously affect the BIT results. Some deviations from this normal configuration have been taken into consideration in the software design. One of these considerations is the inclusion of a 3 dB power splitter in the sum input waveguide to the receiver which is required for test configurations such as acceptance testing and burn-in aging. All other deviations from normal configuration should be avoided if meaningful BIT results are desired.

This document assumes that the tactical software configuration is one of the following:

T258-L
T409-R
T450-J-1S

2.0 BIT MATRIX

This section presents the BIT Matrix. The BIT Matrix consists of two sets of 12 half words in the Radar Data Processor (081) memory which contain BIT test failure data. The two sets of 12 half words are two different BIT matrices which are identical in format.

One of the BIT matrices is called the Continuous Monitor BIT Matrix. This matrix contains the results of BIT tests which are interleaved with radar tactical tasks. These interleaved BIT activities include:

1. System calibrations executed at Major radar operating mode changes
2. Periodic system calibrations executed in Search and Track Modes
3. Periodic tests of the radar acquisition and track capability in the selected tactical mode
4. Periodic checks of R.F. power output
5. Periodic tests of antenna scanning and positioning capability
6. Periodic check sum of the 081 memory to detect memory alterations
7. Results of the 081 and 041 self tests, and 039 A/D converter tests executed at power up
8. Periodic tests of the discrete inputs to the 081 from other LRUs which describe the operational readiness of the radar system.

The remaining BIT Matrix is the Initiated BIT Matrix. This matrix contains the results of the Initiated BIT tests. These tests are executed when the BIT switch on the BIT Control Panel is depressed. The number of tests executed depends on the position of the power switch on the radar control panel (541), and on whether the aircraft is on the ground or in the air (see Table 2.1 below).

TABLE 2.1. ACTIVITIES IN INITIATED BIT

	Power Switch In Standby		Power Switch In Operate	
	Ground	Air	Ground	Air
Optional Track Test			X	X
Clear Initiated BIT Matrix			X	X
Clear Continuous Monitor BIT Matrix			X	
Cycle Paramp	X	X	X	X
VCO, Gain, Phase Calibrations			X	X
Acquisition and Track Tests			X	X
039 Tests			X	X
R.F. Power Tests			X	X
Receiver Blanking Tests			X	X
Range Delay Calibration			X	
Dummy Load Test			X	X
081 Self Test			X	X
041 Self Test			X	X
039 A/D Converter Test			X	X
Antenna Scan Rate Tests (GYRO)			X	
Antenna Scan Rate Tests (TACH)			X	X
Gyro Drift Test			X	
610 Servo Electronics Test			X	X
610 Self Test			X	X
Fault Isolation			X	X
BIT Matrix Readout on VSD	X	X		

As indicated in Table 2.1, the primary purpose of standby initiated BIT is to read out the BIT Matrix on the VSD. The primary purpose on operate Initiated BIT is to execute radar tests. Whenever the Initiated BIT switch on the BIT Control Panel is depressed, the system is under control of the BIT software, and cannot be interrupted from these tasks by the operator except

by depressing reject on the flight control stick. When in the Initiated BIT Mode, the Initiated BIT activities are executed in the order presented in Table 2.1.

Ground/Operate Initiated BIT will execute all the activities indicated in Table 2.1 in approximately 2 minutes if no tests fail. Air/Operate Initiated BIT requires a few seconds less since fewer tests are executed. If some of the tests do fail, the execution time of Initiated BIT could be significantly increased from the nominal 2 minutes. This is because some of the tests are executed 3 times if a failure occurs, but only once if passed, and because the system may fail in such a way that test execution time is increased.

Standby mode Initiated BIT execution time is variable, depending largely on the number of faults discovered in testing. In this Initiated BIT mode the BIT Matrix presented in Figure 2.1 is read out. Each of the 12 BIT Matrix words which contain non-zero data is displayed on the VSD. The format of the display consists of a two character word number, followed by three data characters. Each of the three characters represents four Bits in the BIT Matrix word, so that the three characters represent the entire BIT Matrix word.

Additional information on BIT timing is presented in Section 4.0.

The BIT Matrix read out scheme is programmed to read out only non-zero words, so that three dashes should never be displayed. Each word to be displayed is displayed for 7.5 seconds. The readout is not destructive, so that standby BIT can be re-run, if recording of BIT Matrix data was not successful.

The readout of each BIT Matrix is preceded by a 7.5 second display indicating which matrix readout follows. The display is "I-BIT" for the Initiated BIT Matrix, and "CM-BIT" for the continuous monitor BIT Matrix. The BIT Matrices are read out with the Initiated BIT Matrix preceding the Continuous Monitor BIT Matrix.

At the conclusion of the readout of the Continuous Monitor BIT Matrix, words corresponding to 13 and 14 will display six characters which constitute a program identifier.

The remainder of Section 2.0 presents descriptions of the test which make up the BIT Matrix.

BIT MATRIX

	FIRST				SECOND				THIRD			
MATRIX WORD	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	BIT 9	BIT 10	BIT 11
01 FAULT STATUS	081 FAULT	610 FAULT POWER	041 FAULT	039 FAULT	011 FAULT	001 FAULT	022 FAULT	031 FAULT	610 SERVO FAULT	RDR HOT		PWR/ON SP MEM FAIL
02 RDP STATUS	A&C TEST	RADAR MUX	CC MUX	RSP I/O	AO GROSS	AO SCALE FACTOR	AO LINEAR	ROM CHECK SUM	ENGR FAIL NO. 2	ENGR FAIL NO. 1	CHECK SUM	WATCH DOG
03 RDP STATUS	DO HI GP 0	DO HI GP 1	DO HI GP 2	DO HI GP 3	DO HI GP 4	DO HI GP 5	DO LO GP 0	DO LO GP 1	DO LO GP 2	DO LO GP 3	DO LO GP 4	DO LO GP 5
04 RSP STATUS	041 SELF TEST	039 A/D CONV	PROC SYNC			IDA INTER-RUPT	←		RSP TEST NO. →			
05 RF OSC STATUS	GTWT DRIVE LOCK 1	GTWT DRIVE LOCK 2	GTWT DRIVE LOCK 3	GTWT DRIVE LOCK 4	GTWT DRIVE LOCK 5	GTWT DRIVE LOCK 6	OFFSET LOCK CH 1	OFFSET LOCK CH 2	OFFSET LOCK CH 3	OFFSET LOCK CH 4	OFFSET LOCK CH 5	OFFSET LOCK CH 6
06 RF OSC STATUS	LO POWER CH 1	LO POWER CH 2	LO POWER CH 3	LO POWER CH 4	LO POWER CH 5	LO POWER CH 6	FMR RAMP					
07 XMTR STATUS	RF HPRF 1	RF HPRF 2	RF HPRF 3	RF HPRF 4	RF MPRF	RF LPRF	RF BCN	XMTR SELF TEST	XMTR TIME OUT	COOL/ WG PRESS	D/L OVRD	MULTI-PACTOR FAIL
08	18.4 VCO CALIB	PHASE CALIB	AMP CALIB	RANGE DELAY CALIB	22.8 VCO CALIB	22.8 TRK FREQ	BCN LO		18.4 TRK FREQ	A/D CONV BAL	AMPL CALIB PA	AMPL CALIB PA
09 RCVR TGT	VS SB 1 SENS	VS SB 2 SENS	RWS SENS	HPRF TK	BLANK GATE	NET 2			MPRF GAIN BAL		HPRF GAIN BAL	
10 ANT. TGT	MPRF SENS	LPRF SENS	BCN SENS	TRK SIG LEVEL					AZ PSD	EL PSD	TACH MODE	GYRO MODE
11 ANT. STATUS	ANT. IN POS	AZ GYRO DRIFT	EL GYRO DRIFT	SCAN RATE	ROLL RATE	AZ/EL DIODE FAIL	AZ SERVO ELECT	EL SERVO ELECT	ROLL SERVO ELECT	RE-SPONSE TIME	SCALE FACTOR	ZERO BAL-ANCE
12	001 FAULT INDIC	011 FAULT INDIC	022 FAULT INDIC	031 FAULT INDIC	039 FAULT INDIC	041 FAULT INDIC	RDR HOT SYS FAULT	PWR/UP SP MEM FAIL	610 FAULT INDIC	GBIT RUN	ABIT RUN	ANT. TEST BYPASS

Figure 2-1. BIT matrix.

TABLE 2.2. DECODING BIT MATRIX CHARACTERS

Character Displayed	Code	Character Displayed	Code
–	0000	H	1000
A	0001	I	1001
B	0010	J	1010
C	0011	K	1011
D	0100	L	1100
E	0101	M	1101
F	0110	N	1110
G	0111	O	1111

2.1 UNIT FAULTS (WORD 1, BITS 0 – 8)

The objective of the BIT tests is to detect a radar system failure, and to isolate that failure to the faulty unit. The unit faults in the BIT Matrix contain the results of that fault isolation. Setting of any of the unit faults in the BIT Matrix will result in setting the unit fault annunciator on the various units. These fault annunciators are set when the system is in Initiated BIT, Power Up, or Shutdown.

The BIT Matrix unit faults may be set in two ways:

1. By failing a test which directly isolates to a unit
2. By a deductive process which examines the pattern of test failures to isolate to a unit.

2.1.1 Direct Fault Isolation

Several of the BIT tests involve only one LRU. Failure of these tests will result in direct fault isolation to that LRU and simultaneous setting of the unit fault in the BIT Matrix. These failures are called direct fault isolations because the test failure can be attributed to a particular unit independent of other system failures. Because these tests are executed as stand-alone LRU

tests, it is possible in these cases for BIT to declare more than one unit faulty. The direct fault isolation tests are listed below:

1. 081 Fault. Direct isolation to the 081 will result from failure of any or all of the following tests:
   a. 081 Arithmetic and Control Test
   b. Radar MUX Test
   c. RSP I/O Test
   d. Analog Output Gross Test
   e. Analog Output Scale Factor Test
   f. Analog Output Linearity Test
   g. Checksum Test
   h. Watchdog Interrupt Test
   i. Discrete Output Tests
   j. Radar Overheat
   k. Energizer Test
   1. Scratch Pad Memory Fault.
2. 610 Fault Power. Direct fault isolation to the Low Voltage Power Supply (610) will result if the 610 does not send a 610 operational signal to the 081 despite three attempts to turn the 610 on
3. 041 Fault. Direct isolation to the 041 will result from failure of any or all of the following tests:
   a. 041 Self Test
   b. Loss of Process Sync Interrupt
   c. Loss of IDA Interrupt
4. 031 Fault. Direct isolation to the 031 will result from failure of an Initiated BIT antenna test, if the 610 servo electronics tests pass.

   Direct isolation to the 031 will result if the Az/El diode test fails
5. 610 Servo Fault. Direct isolation to the 610 will result from failure of the 610 servo electronics tests in Initiated BIT.

2.1.2 Deductive Fault Isolation

Most of the BIT tests require proper operation of more than one LRU. Therefore, a failure of any one of these tests does not by itself uniquely isolate to a faultly LRU. Very often however, a breakdown of some component

in an LRU will result in failures of more than one BIT test. Examination of the pattern of BIT test failures can result in correct fault isolation to that LRU. Alternatively, a breakdown of some component in an LRU perhaps should result in failure of a particular BIT test. If the test does not fail, it can be inferred that the component under consideration is not faulty. Thus, in the deductive fault isolation process, conclusions are derived from which tests fail, as well as tests which do not fail.

The deductive fault isolation process assumes that only one LRU is faulty. This assumption is made because it is too difficult to isolate multiple failures by deduction. The only reasonable method of isolating more than one failure to more than one LRU is to devise direct isolation tests for each LRU; this solution was not considered feasible if the radar set was to have another mission besides fault detection and fault isolation.

The primary impact of the single fault assumption is that the deductive fault isolation process stops as soon as a unit fault is declared. Therefore, if multiple faults exist, BIT deductive fault isolation will only isolate to one LRU. Before the second faulty unit can be isolated, the first faulty unit must be repaired or replaced.

Figure 2.1.2-1 presents the logical structure of the BIT deductive fault isolation. Deductive fault isolation is divided into two parts. Part I is executed at shutdown and in Initiated BIT. Part II is executed only in Initiated BIT.

The difference between the two parts is that Part I consists of deductions resulting from tests which are very nearly direct isolation tests, so that unit faults can be assigned on the basis of test failure alone.

Part II consists of deductions drawn from the pattern of failures, i.e., which tests did not fail, as well as which tests did fail. In order to be able to draw a conclusion from which tests did not fail, the deductive logic must assume that the test was executed. Since there is no guarantee that all tests have been executed except in Initiated BIT, Part II of the deductive fault isolation is executed only in Initiated BIT.

In reading the following on deductive fault isolation, it is recommended that frequent reference be made to Figure 2.1.1-1, and Figure 2.1.2-1.

ALTERNATE MAINTENANCE GUIDE

(USE ONLY WHEN BIT FAULT ISOLATION IS INSUFFICIENT)

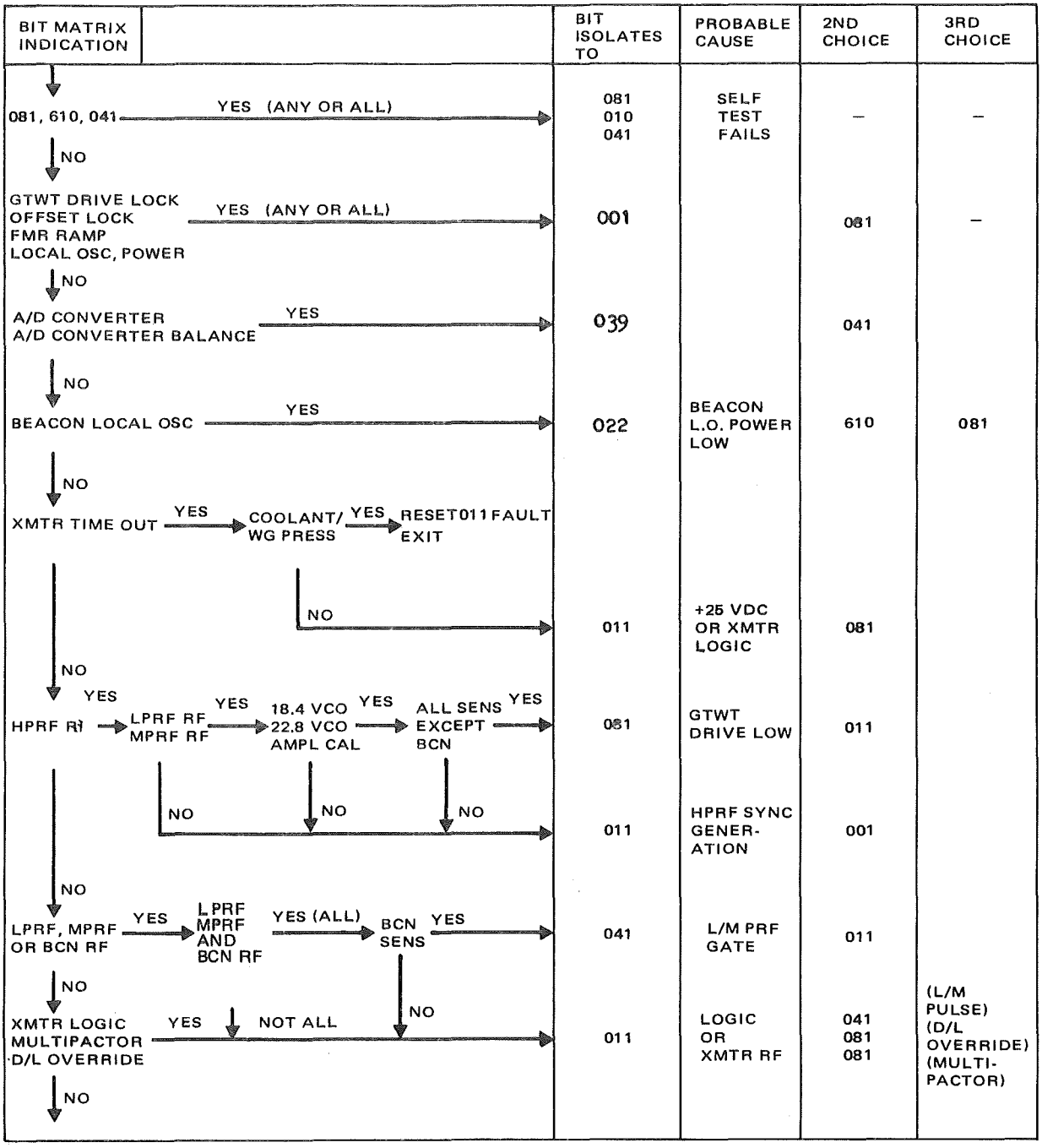

Figure 2.1.1-1. BIT fault isolation.

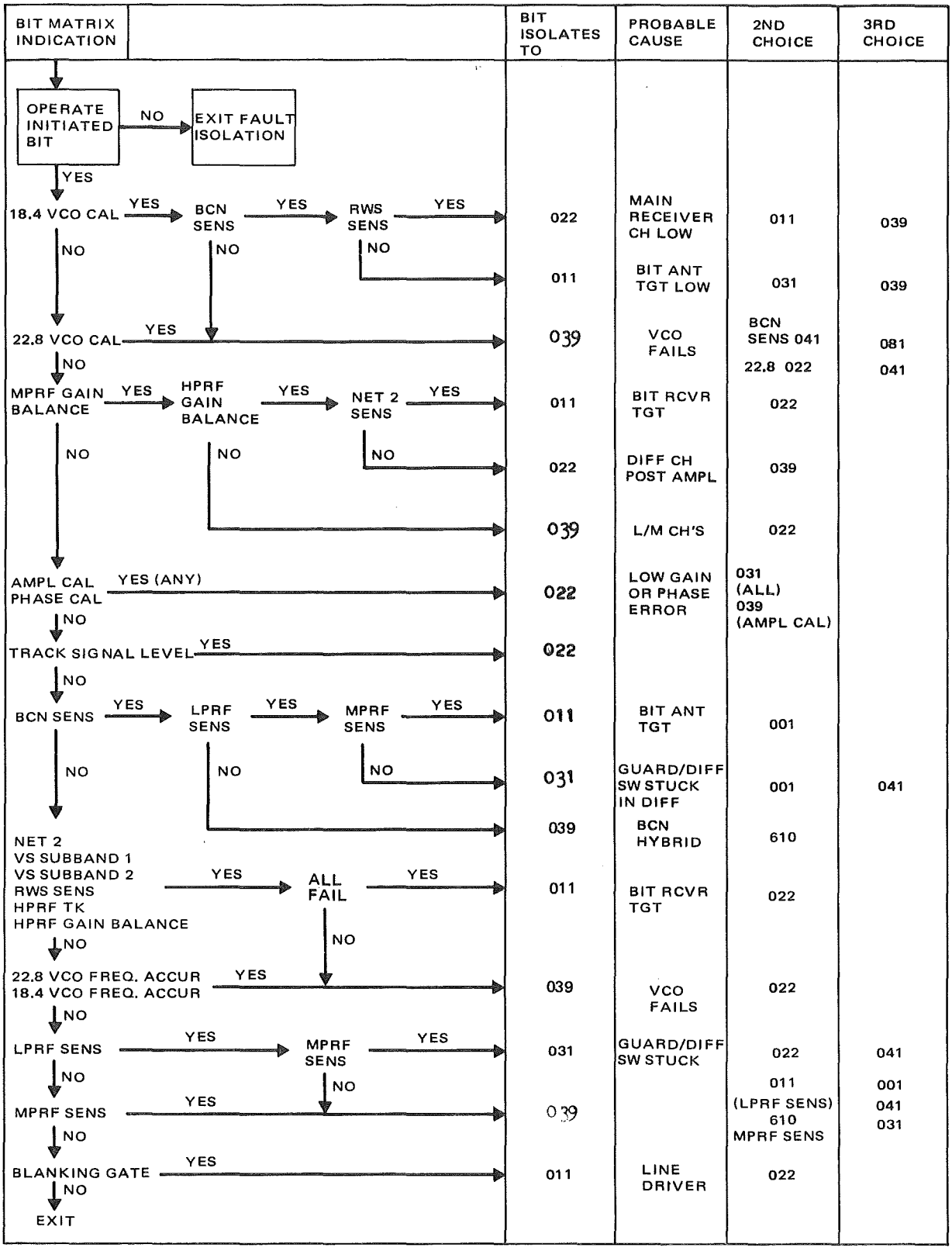

Figure 2.1.2-1. BIT fault isolation

2.1.2.1 Deductive Fault Isolation – Part I

Part I of the Deductive Fault Isolation begins by checking the BIT matrix for faults in the 081, 041, or 610 units detected by the Direct Isolation tests. If any of these units have been faulted, no Deductive Fault Isolation is attempted. The Deductive Fault Isolation is halted because without a good 081, 041, and 610, no credence can be placed on other test failures. Therefore, until these units are deemed adequate no further fault isolation is attempted.

Exciter Faults. Assuming that the 081, 041 and 610 have passed Direct Isolation Tests, the Deductive Fault Isolation then checks for Exciter Signal Test failures, GTWT Drive Lock, Offset Lock, L.O. Power, and FMR Ramp. If any of these have failed, the exciter fault is set in the BIT matrix. These Exciter Test failures are checked early in the Deductive Isolation process because it is important that the exciter is producing a stable signal at the proper frequency if any credence is to be placed on other test failures.

039 A/D Converter Fault. The next check is for a good 039 A/D converter. This device converts all the radar signal data from analog to digital form. All of the acquisition tests, track tests, and calibrations require a functional 039 A/D converter to pass.

Two 039 A/D converter tests are made in BIT. They are the 039 A/D Converter Test (Word 4, Bit 1), and the 039 A/D Converter Gain Balance Test (Word 1, Bit 9). The first test is a check on the fidelity of the A/D conversion, and the second test is a check on the gain balance of the outputs of the A/D converter, given equal inputs.

Failure of either test results in fault isolation to the 039 unit.

Beacon L.O. Fault. If the exciter tests and 039 A/D converter tests have passed a check is made for the Beacon L.O. fault in the BIT matrix. This fault results in a 022 fault. Note that the exciter A/D converter and Beacon L.O. checks are for all practical purposes Direct Isolations.

Transmitter Time Out Fault. The next check is for the transmitter time out fault in the BIT matrix. If transmitter time out failure is indicated, BIT then checks the coolant flow rate fault in the BIT matrix. If the coolant fault is set, the transmitter time out fault is assumed to have been caused by

lack of sufficient coolant flow. Since the coolant flow problem is not a transmitter problem, no transmitter fault is set, and the Deductive Fault Isolation proceeds to Part II because the remainder of Part I includes power checks which cannot be expected to pass without transmitter time out.

If the transmitter time out fault is set in the BIT matrix, but the coolant fault is not, the transmitter is declared the culprit.

RF Power Faults. If the 011 time out fault is not set in the BIT matrix, a check is made for HPRF Power Faults in the BIT matrix. A HPRF power fault immediately throws suspicion on the transmitter. Before tagging the transmitter, however, the Deductive Fault Isolation logic makes a check for low GTWT Drive Power; for this could also result in a HPRF power fault. The test for Low GTWT Drive Power is made by checking the BIT matrix for all tests which use the GTWT Drive. If all such tests have failed, it is a good bet that the HPRF power failure was caused by a weak GTWT drive, so the exciter is tagged. If any tests which use the GTWT drive have passed, the HPRF power fault is assigned to the transmitter.

Note that before the exciter can be faulted because of low GTWT drive power, all tests using the GTWT drive must be faulted in the BIT matrix. This means that if any of the tests have not been executed (as they might not unless the Deductive Fault Isolation is being executed in connection with Initiated BIT), a HPRF power fault will be assigned to the 011.

If the HPRF power tests have passed, BIT proceeds to check the MPRF, LPRF, and Beacon power faults in the BIT matrix. If any of these tests fail, the transmitter is suspect. BIT then checks to see if all three (MPRF, LPRF, Beacon) power tests have failed. If they have not all failed, the fault is isolated to the transmitter. This isolation is probably a defective GTWT in HPRF or LPRF, or a defective beacon magnetron. If the MPRF, LPRF and Beacon power tests have all failed, there is a good chance that the 041 pulsing trigger is missing. To verify this, a check is made for a Beacon acquisition test fault in the BIT matrix. If the Beacon acquisition test had passed, the 041 trigger must have been present, so the MPRF, LPRF and Beacon power failures are probably due to a fault in the 011 Grid modulator circuit; BIT assigns the fault to the 011. If the Beacon acquisition test also

failed, the 041 pulsing trigger is almost certainly missing, and BIT tags the 041. As before, the deductive Fault Isolation assumes that the Beacon acquisition test has been executed. If not, BIT will isolate to the 011.

Dummy Load and Multipactor Faults. If none of the power tests have failed, the BIT matrix is searched for a dummy load, multipactor, or 011 self test fault. If any of these tests have failed, the 011 is tagged.

2.1.2.2 Deductive Fault Isolation – Part II

This part of the Deductive Fault Isolation is executed only in Initiated BIT because conclusions cannot be drawn unless all tests have been executed. In all cases this deductive logic will isolate one unit. In each case, the isolated unit is the most probable faulty unit as determined by a system study, as well as a survey of field reports.

Also, in some cases, alternate choices are presented. In each case an attempt has been made to indicate the level of confidence in the primary and secondary fault isolations.

18.4 VCO Calibration Fault. Part II begins by checking the BIT matrix for an 18.4 MHz VCO calibration fault. If there is a fault, the deductive logic checks for a Beacon Acquisition test fault. The Beacon Acquisition test can be passed even though the 18.4 MHz VCO does not calibrate properly. Therefore, if the Beacon Acquisition test did pass, the calibration fault is probably what it appears to be, a failure of the 039 to properly execute the calibration. The deductive logic will fault the 039. The second and third choices are the 041 and the 081. This is because the command to calibrate the VCO originates in the 081, and is passed on to the 039 by the 041. Thus, any break in the command chain would cause a 18.4 MHz VCO calibration fault.

If the Beacon Acquisition test failed along with the 18.4 MHz VCO calibration fault, the probability is that the calibration fault resulted from failure of the antenna target to reach the 039. To determine why the target was lost, a check is made for RWS acquisition test fault in the BIT matrix. The RWS test has the largest failure margin of any of the BIT test which uses the receiver target. Therefore, if the RWS test also failed, it appears that both the antenna and receiver targets are missing. This might point to a low

GTWT drive power, but the fact that the power tests passed in Part I of the Deductive Fault Isolation precluded that possibility. The most probable cause, then, is low main channel gain in the 022; BIT thus isolates to the 022. Another less probable cause is the loss of both targets due to faulty gating circuits in the 011.

If the RWS test passes, then the situation is that the 18.4 calibration and the Beacon Acquisition test failed, but RWS passed. The two failures point to loss of target, but passing the RWS test indicates that the 022 main channel is OK. BIT, therefore, isolates to the 011; the presumption is that the 011 is not producing the antenna target. The second choice is that the antenna target is somehow lost in the 031.

22.8 MHz VCO Calibration. A failure of the 22.8 MHz VCO calibration is assigned to the 039. This assignment is made for two reasons. First, and most important, the most probable cause is a failure of the 22.8 MHz VCO, which is resident in the 039 unit. The second reason is BIT has little other information on which to deduce another faulty unit.

MPRF Gain Balance. The next check made is for a MPRF Gain Balance failure. When this test fails, the fault is very likely in three units – the 039, 022 or 011. To isolate correctly among these units, the deductive logic checks the HPRF Gain Balance Test. Both the HPRF and MPRF Gain Balance tests use the same circuits in the 022 and 011 units. Thus, if the HPRF Gain Balance test passes, the failure of the MPRF Gain Balance test must result from a fault in the 039. In such a case the fault must be in the LPRF/MPRF circuits of the 039.

If the HPRF Gain Balance test also fails, the fault probably is upstream of the 039. This is because the MPRF and MPRF Gain Balance tests use different circuits in the 039 downstream of the 30 MHz band pass filters. Therefore, to assign the fault to the 039 would require an assumption of two different faults in the 039. This possibility is considered more remote than a single fault in the 011 or 022 units. There is a possibility that there could be a fault in the 30 MHz filters of the 039 unit which are commonly used by both tests; these circuits have been quite reliable, however, so that a 30 MHz filter fault in the 039 is at best a second choice.

With the suspicion that the fault is in the 011 or 022 units, the fault isolation logic checks the NET2 test to try to isolate further. The NET2 test is selected because only a functional main channel in the 022 unit is required to pass this test, assuming there is a signal input (receiver target) from the 011 unit. If the NET2 test passed, it can be concluded that the target is present, and that it is not significantly attenuated. The latter conclusion can be drawn because the NET2 test is the most sensitive of the receiver target tests to absolute signal level. The passing of the NET2 test thus indicates the presence of a strong receiver target; this clears the 011 unit, since its only function in these tests is to produce the target. Having cleared the 011 unit, this combination of faults, i.e., MPRF Gain Balance – Fail, HPRF Gain Balance – Fail, and NET2 – Pass, is probably due to low gain in the difference channel of the 022. Since both tests which failed use the same receiver circuits up through the 90^{o} track hybrid, the most probable location of the fault is the 022 difference channel post amplifier. As noted above, a second choice is the difference channel 30 MHz bandpass filter in the 039, but this is considered more remote than a 022 fault.

If the NET2 test had also failed suspicion would be cast on the 011 unit. In this case the most probable cause is a missing, or significantly attenuated receiver target – fault the 011.

Amplitude of Phase Calibration Fault. If the MPRF Gain Balance test passed, the deductive fault isolation logic looks for either a phase balance calibration fault, or an amplitude calibration fault. A fault from either of these calibrations will result in tagging the 022 unit, but for different reasons.

A Phase Balance Calibration failure is assigned to the 022 unit primarily because the bulk of the phase balance circuitry is in the 022 unit, thus it is the most probable unit at fault. A second choice is the 081 unit which commands the channel balance – possibly the command never got to the receiver. A third more remote possibility is that the 041 never commanded the antenna to switch from Main/Guard configuration to the Sum/Difference configuration. A fourth choice of the antenna is even possible; maybe it did not respond to the 041 command.

Like the Phase Calibration fault, the Gain Calibration fault is also assigned to the 022 unit. In this case there is almost no other choice. In order to get to this point in fault isolation, the 041 Self Test must have passed, eliminating the remote possibility that the 041 might be at fault. Also to get to this point in fault isolation, the MPRF Gain Balance must have passed; this clears the 039 of producing the gain imbalance between channels. The only other place where the gain imbalance could be introduced is in the 022 unit. Therefore, BIT assigns a Gain Calibration fault to the receiver.

There still exists a possibility that Gain Calibration fault could be the result of some antenna malfunction in producing the target signal for calibration, but this choice is definitely less probable.

MPRF Track Signal Level Fault. Failure of the MPRF Track Signal Level test is assigned to the receiver. This conclusion is largely based on tests which have not failed to this point. The fact that to get here both phase and amplitude calibration must have passed indicates that the antenna target is alive and well. Passage of the MPRF Gain Balance test indicates that the signal processing chain from the 039 downstream is OK. The only choice left is the receiver, there is no reasonable second choice.

Beacon Acquisition Fault. The BIT matrix is next searched for a Beacon Acquisition Fault. If there is a Beacon Acquisition Fault, a check is made for a LPRF acquisition fault. Since the Beacon and LPRF tests are nearly identical except for the 039, failing Beacon Acquisition and passing LPRF Acquisition almost certainly indicates that the 039 Beacon channel is bad. BIT faults the 039. Alternate choices of 610 and 081 are considerably less probable.

If both the LPRF and Beacon Acquisition tests fail, the fault isolation logic is in some difficulty. At this advanced point in the deductive isolation problem, this should not happen. The MPRF Gain Balance and MPRF Track Signal tests have passed, indicating good gain balance in the analog signal processing chain. The 041 self test has passed, indicating good digital signal processing. The amplitude calibration has passed indicating good absolute signal level in the antenna target. The amplitude calibration is the most sensitive of the antenna target tests to absolute target level.

For completeness, the fault isolation logic makes a stab at picking an LRU other than the 039, but either choice of 011 or 031 is improbable. The basic point to be made here is that the fault isolation logic will rarely, if ever, get to this point, so even if its wrong, little of any serious consequence could result.

Receiver Target Faults. The BIT matrix is next examined for faults which are sensitive to the absolute magnitude of the receiver target. These are the NET 2, VS Sub Band 1 and 2, RWS, HPRF Track, and HPRF Gain Balance tests. If all of these tests fail, the problem is almost certainly a significantly attenuated receiver target. This fault is assigned to the 011 where the receiver target is produced.

If only some of these tests fail, the fault is assigned to the 039 on the assumption that the overall gain is low. A strong second choice in this case is the 022 for similar reasons.

22.8 MHz or 18.4 MHz VCO Frequency Accuracy. Failures of these tests are almost certainly due to sub-par VCOs. The VCO in question is probably faily good, since, to get here, the VCO calibration must have passed. These tests are more stringent in positioning precision, so that it is possible that the VCO calibrations could pass, and one of these tests fail. Since the VCOs reside in the 039 unit, this fault is assigned to the 039.

LPRF Acquisition Fault. The deductive fault isolation logic proceeds to check BIT Matrix for a LPRF acquisition fault. If the test failed, the target must be missing. The MPRF acquisition test is checked. If it also failed, BIT tags the 031 on the presumption that the antenna diode switch is stuck in the difference position. If the diode switch is stuck in the difference position, the 041 will interpret the difference signal (which now carries the antenna target) as the guard signal. The target will then fail to pass main/guard ratio, resulting in a lost target. An alternate choice is that the pulse compression code is not being properly received by the 011.

If the LPRF test fails, but the MPRF acquisition test passes, the problem probably arises from a fault in the LPRF circuits in the 039. The second choice, 610 unit, presumes that some sort of ripple in what should be a DC voltage from the power supply caused the LPRF fault. About all that can be said for this choice is that it happened once. The third choice, no

LPRF target somewhat remote since the Beacon test which uses the same target did not fail.

MPRF Acquisition Fault. If the LPRF test passes, the MPRF test is checked. A failure here is probably low 039 gain.

Blanking Gate Fault. If MPRF test passes, the blanking gate fault is checked for in the BIT Matrix. To get to this point in the fault isolation, the VS Acquisition test must have passed. If the VS test passes and the Blanking Gate test fails, the fault is surely in the blanking gate circuit. BIT assigns the fault to the 011, because experience indicates that the circuits in the transmitter are more often at fault. The alternate choices of receiver blanking circuits and poor connection between the 011 and 022 are more than plausible.

If no blanking gate fault exists in the BIT matrix, fault isolation is over. With the exception of range delay calibration any fault in the BIT matrix should result in isolation to a unit. The range delay calibration has been omitted, because it is difficult to envision a fault which would result only in a range delay failure.

2.2 RADAR DATA PROCESSOR TESTS

2.2.1 Arithmetic and Control Test (Word 2, Bit 0)

This test is designed to exercise the arithmetic and control logic of the Radar Data Processor (081). The ability of the 081 to execute the Program instructions is tested; the ability of the 081 to process an interrupt is tested.

The arithmetic test of program instructions is accomplished by performing a series of arithmetic computations. The series of instructions is programmed to use as many different instructions as possible. For example, a constant from the memory might be loaded into a general purpose register (GPR) multiplied by another constant, divided by a third constant, inverted in sign, stored in memory, and retrieved into a different GPR. The result of all these operations might then be compared to the known result to establish pass or fail. If the results match the known result, the test has established

to capability of the computer to properly execute the specific instructions in that chain. If the results do not match the known result, some instruction in that chain was not executed properly, and the test fails.

The sequence of instructions in the example above is not one that is executed as a part of this test, and is presented only to illustrate the test philosophy. The actual sequence of instructions used for this test executes 87 of 91 possible program instructions. Of the four untested instructions, two (PCW and LCW) are Input/Output instructions which are extensively tested as a part of the 081 Multiplexer tests. One of the untested instructions, the BIT instruction, is partially but not completely tested as part of the multiplexer tests, and the remaining instruction, the AGE instruction, is not used in the tactical program.

The control test checks the ability of the 081 to successfully process an interrupt. Since some of the interrupts are generated outside the 081, these cannot be tested; only the arithmetic anomaly, illegal write, and A/D/A conversion interrupt are generated and tested.

The control test consists of generating the three interrupts with the tacticals interrupts disabled. The tactical interrupts are then enabled, at which time the arithmetic anomaly interrupt (which has the highes priority of the three) is honored. A check is made for a proper return address for this interrupt. If the return address is not correct, the control test fails. Assuming a correct return address, the tactical interrupts are again enabled. The tactical interrupts are automatically disabled when any interrupt is honored. Enabling the tactical interrupts will allow honoring the next priority interrupt, illegal write interrupt.

After some bookkeeping to indicate that the second interrupt was honored, the tactical interrupts are enabled again. A check is then made to ensure that all three interrupts had been honored, and that all three interrupts were honored in priority order. If these criteria are not met, the control test fails.

The arithmetic and control tests are executed as part of the 081 self test, which is executed at power up, during Initiated BIT, and when recovering from a long transient. The arithmetic and control tests are executed

three times on every execution of the 081 self test. If either the arithmetic test or program instructions or the control test of interrupts fails, a fault for the entire test is logged. If a fault is recorded on all three tries of the arithmetic and control test, and A&C fault is recorded in the BIT Matrix, a 081 fault is recorded in the BIT Matrix, and a NoGo is sent to the BIT Control Panel.

The arithmetic and control test requires about 10 milliseconds for each execution.

2.2.2 Radar Multiplex Terminal Test (Word 2, Bit 1)

The radar multiplex terminal is variously called the R-MUX, P-MUX, and Radar MUX. In tactical radar operating mode, this unit is used to:

1. Transmit RSP and DSC commands from the Radar Data Processor (081) to the Digital Signal Processor (041)
2. Receive data from the Inertial Navigation System (INS) or Attitude-Heading Reference set (AHRS).

As an independent unit of the 081, the radar multiplex terminal has the capability of directly accessing the 081 memory. This capability is used to receive or transmit data from reserved memory cells allocated for the exclusive use of the Radar Multiplex Terminal. These reserved memory cells are divided into eight blocks of sixteen words each. A single data message either to or from the 081 through the radar multiplex terminal must be completely contained in at most 15 of the 16 words of any data block. Thus, the maximum allowable message is 15 words. In current tactical usage only two of the eight data blocks are used, and the maximum message lengths are fifteen 24 bit words for the RSP/DSC data, and six — 16 bit words for the INS/AHRS data.

To initiate a transmission from the 081 to the 041 through the radar multiplex terminal, the software is programmed to store the RSP data to be transmitted into the reserved memory cells, and to execute a PCW instruction. The PCW instruction causes the radar multiplex terminal to generate a data initiate signal to the 041 and to gain control of the 081 main bus, and

convey the data stored in the reserved memory cells to a 25 bit register called the serial data register. The data is sent into the serial data register in parallel. Once in the serial data register, the data word is shifted circularly to the appropriate position in the serial data register, then transmitted in serial form to the 041 unit. After the word has been transmitted, the next word in the message is acquired from memory, and the process repeated until the entire message of up to 15 words is transmitted. After the complete message has been sent, the radar multiplex terminal generates a completion interrupt.

Reception of a message through the radar multiplex terminal is the reverse of transmission. The PCW instruction is data output from the 081. The PCW command causes the radar multiplex terminal to send a data initiate request to the INS or AHRS. The requested data is then sent in serial form to the serial data register. Once in the serial data register, the data is shifted to the appropriate position in the register, then shipped in parallel to memory. After all words of message have been transmitted, a completion interrupt is generated.

To test the operation of the radar multiplex terminal special BIT test circuits have been incorporated. These test circuits cause the output of the serial data register to be disconnected from the outside, so that no data is transmitted or received from outside the 081. The BIT test circuits are activated when the software executes a PCW instruction in BIT format.

There are three Radar Multiplex Terminal tests. They are:

1. Test for parity error
2. Test for data error
3. Test for good data transmission.

Parity Error In tactical operation all data entering the serial data register from outside the 081 is encoded with odd parity. If the received data does not have odd parity, a program error interrupt is generated. The parity error test purposely creates a parity error, and checks to see if the error interrupt was generated to verify detection of the parity error.

To create the parity error, the serial data register is first loaded with a known constant. Then using the PCW instruction, the radar multiplex terminal is configured to receive data into one of the sixteen word data blocks of memory not used by the tactical program. The PCW instruction is issued in BIT format so that no data is actually received from outside the 081. The constant in the serial data register is shifted circularly, checked for parity, and shipped to memory if the parity is odd. If the parity is even an error interrupt is generated, and the even parity word is not shipped to memory. The constant in the serial data register is then circularly shifted again for the next word. This process is repeated until fifteen circular shifts corresponding to 15 words have been executed, and thus fifteen parity checks have been made. The constant pre-loaded into the serial data register is selected so that the circular shifts will always result in at least one of the fifteen words containing even parity.

After the completion interrupt the BIT software checks the interrupt register to verify that a parity error had been detected. If a parity error had been detected, the test passes, if not the radar multiplex terminal test fails.

Assuming that a parity error had been detected, the BIT software then sums the fifteen words received in this test. The sum is checked against a constant. If the sum is not equal to the constant, the test fails. If it passes, the radar multiplex test proceeds to the data error detection test.

Data Error The 081 is equipped with special BIT circuits to test the data error detection capability of the radar multiplex terminal. This BIT circuitry will generate a data error whenever an attempt is made to receive data into block 0, using a PCW instruction in BIT format. If a data error is detected, an error interrupt is generated and no data is shipped to memory.

This test consists of generating the data error in the manner described above, and checking to see if the error interrupt was generated. If it was, the test passes, and if not, the radar multiplex test fails.

If the data error was detected, an additional check is made to see if the contents of the serial data register were shipped to memory. Because of the data error, the contents of the serial data register should not have been

shipped. The test fails if the receive word is altered during this part of the radar multiplex test. If the word is not altered, the test passes, and the good data transmission test is executed.

Good Data In this test, an attempt is made to load the serial data register with good data, using the PCW instruction in BIT format. If the data is transmitted with no error interrupt, the test passes; otherwise it fails. If it passes, a check is made of the contents of the serial data register to verify that the correct word was transmitted. If the contents are not correct, the test fails. If the test passes, the radar multiplex test is complete.

The radar multiplex test is executed as a part of the 081 self test, which is executed at power up, when recovering from a long transient, and in Initiated BIT. On each execution of the 081 self test, the radar multiplex test is executed three times. If the radar multiplex test fails all three times, a radar MUX fault is set in the BIT matrix, a 081 fault is set in the BIT matrix, and a NoGo is sent to the BIT control panel.

The radar multiplex test requires about 2 milliseconds for execution.

2.2.3 Central Computer Multiplex Terminal Test (Word 2, Bit 2)

The Central Computer Multiplex Terminal, also known as the C-MUX, is the connecting link between the radar data processor (081) and the central computer. As such, the C-MUX passes all data between the radar data processor and the central computer.

In tactical radar operation, all messages transmitted between the 081 and the central computer are initiated by the central computer. Data transmissions are initiated when the central computer sends a data initiated word called the select word to the C-MUX. The select word is encoded to indicate the mssage type (input or output), and the message length. The C-MUX then gains control of the 081 main bus, and as an independent unit of the 081, communicates directly with the 081 memory.

A BIT test of the C-MUX requires the capability to transmit data through the C-MUX. Since the data transmission is normally initiated by the central computer, which is external to the radar, some means must be devised to initiate data transmissions through the C-MUX entirely within the 081.

This is done by activating special BIT circuits within the 081 which connect the C-MUX input to the radar multiplex terminal output. Then, a test of the C-MUX can be made be sending a data initiation select word through the radar multiplex terminal to the C-MUX. This can be followed by a test message. The special BIT circuits which connect the C-MUX to the Radar Multiplex Terminal can be activated by the software using a special form of the BIT instruction.

There are three BIT C-MUX tests. They are:

1. Parity error detection
2. Data error detection
3. Good data transmission.

Parity Error. For this test, C-MUX is connected to the radar multiplex terminal. The radar multiplex terminal is pre-loaded, then commanded to output a two word message. The command to the radar multiplex terminal is issued in the BIT format, so that no data is actually output from or input to the 081. The message output from the serial data register has the correct select word for CCC message 6, so that any data entering the C-MUX from the radar multiplex terminal should be stored in the 081 memory cells reserved for that CCC message if and only if no errors are discovered in the data. If an error is discovered in the data, that word is not transmitted to the 081 memory, so that the corresponding memory cell should remain unchanged.

One type of error which might be detected is a parity error. All data words transmitted by the central computer should be encoded with odd parity. If the word received by the C-MUX has even parity, that word is discarded.

This test then consists of sending a correct select word, then sending a data word with even parity. Time is allowed for completion of the message transmission (180 microseconds), then a check is made for a C-MUX message complete interrupt. If the interrupt is not there, the parity error test fails.

Assuming that the C-MUX message complete interrupt is there, the BIT software then makes a check of the 081 memory to verify that the word containing the parity error was not transmitted. If the memory cell is

changed through the test, the C-MUX parity detection test fails. If the memory cell is unchanged, the parity detection test passes, and the C-MUX test continues to the data error detection test.

Data Error. The radar multiplex terminal is then commanded to output a 24 bit word from the serial data register. The serial data register has been pre-loaded so that the first 16 bits form a proper select word. The C-MUX is equipped to accept only 16 bit words, so that after the first 16 bits constituting the select word have been transmitted the C-MUX would expect a 5 microsecond pause, followed by a 16 bit data word. Instead the radar multiplex terminal continues sending data until all 24 bits are sent. The C-MUX interprets the 24 bit word as a 16 bit select word, 5 microsecond pause (at one bit per microsecond), followed by a three bit data word. The data word expected is 16 bits long, the word received is only 3 bits long. This will be interpreted by the C-MUX as data drop out error, and the data word should not be transferred to the 081 memory. The BIT software checks to see that the data was not transferred to memory. If it was transferred, the data error test fails. If not, the C-MUX test proceeds to the good data test.

Good Data. In this test, a proper select word is followed by a valid length data word in the correct parity. This data should be transferred to memory. If it is not, the good data test fails. If it is, the C-MUX test is complete, and has passed.

The C-MUX test is executed as a part of the 081 self test, which is executed at power-up, during Initiated BIT, and when recovering from a long transient. On every execution of the 081 self test, the C-MUX test is executed three times. If any one of the three parts (parity error, data error or good data) of the C-MUX test should fail on any of the three executions of the C-MUX test, a C-MUX fault is set in the BIT matrix, a 081 fault is set in the BIT matrix, and a NoGo is sent to the BIT Control Panel.

The C-MUX test takes about 2 milliseconds to execute.

2.2.4 RSP Special Unit Test (Word 2, Bit 3)

In tactical radar operation the RSP special unit acts as the interface unit of the 081 which receives signal processing data from the 041. The data is transmitted to the 081 by the Interface Data Assembler (IDA) unit of the 041.

A data transaction is initiated by the 041 unit by sending a data valid signal to the 081. The reception of the data valid signal by the 081, causes the RSP Special unit to automatically transfer signal data from the 041 IDA unit directly to the 081 memory. Each data transaction through the RSP special unit consists of 30 twelve bit words. A completion interrupt (the so-called IDA interrupt) is issued by the RSP special unit at the conclusion of the 30 word data transaction.

In order to test the RSP special unit, BIT circuits have been designed into the 081. The BIT circuits, which are activated under software control, accomplish the following:

1. Place the RSP Special unit in BIT mode, disconnected from the 041
2. Initiate a data valid signal to simulate the data valid signal generated from the 041 tactically
3. Transmit a pre-assigned data pattern to the 081 memory.

For this test, the action of the BIT software is to activate the RSP Special unit BIT circuits using the BIT instruction in the appropriate format. The hardware BIT circuits then accomplish the three steps noted above. The RSP special unit follows the transaction with a completion interrupt.

Following the completion interrupt, the BIT software checks the 081 memory to verify that the pre-assigned data pattern was transmitted correctly. The check consists of summing the thirty half-words and comparing the sum to a known result. If the comparison agrees, the test passes. If not, the test fails.

The RSP special unit test is executed as a part of the 081 self test. The 081 self test is executed at power up, during Initiated BIT, and when recovering from a long transient. On each execution of the 081 self test, the RSP special unit test is executed three times. If the RSP special unit test fails on all three executions of the 081 self test, an RSP I/O fault is set in the BIT Matrix, a 081 fault is set in the BIT matrix, and a NoGo is sent to the BIT Control Panel.

The RSP special unit test is executed in less than one millisecond, or next to nothing flat.

2.2.5 Analog Output Tests

There are nine analog output (AO) channels from the data processor (081). They are listed below:

AO Number	Signal Name	Receiving Units	
0	Spare*		
1	Spare*		
2	AO Monitor	081	
3	Azimuth Drive Command	610	
4	Elevation Drive Command	610	
5	Roll Drive Command	610	
6	Radar Range Rate	Armament Control System	Not Tested
7	Radar Range Rate	Lead Computing Gyro	
8	Radar Range	Lead Computing Gyro	

*These signals have been deleted on 081 units S/N 13 and above.

The purpose of the AO tests is to verify the ability of 081 to apply voltages on the AO lines. This verification consists of four tests, the A.O. scale test, the A.O. gross test, the A.O. individual test, and the Analog/Digital/Analog (A/D/A) Converter Linearity test.

The AO's numbered 6, 7, 8 are not tested due to a procurement specification requirement that no invalid signals should be sent to the avionics during BIT.

The A.O. Test is executed as a part of the 081 self test. The 081 self test is performed during initiated BIT, at power up, and when recovering from a long transient. The A.O. Test is executed three times on every execution of the 081 self test. Should an A.O. Fault be set in the BIT matrix, a radar NoGo is set, and a 081 fault is recorded in the BIT matrix. The 081 fault will eventually result in setting the 081 fault indicator.

1. A.O. Scale Test (Word 2, Bit 5) — This test is designed to check the 10 volt reference voltage which is used to scale the analog outputs in the A/D/A converter. An analog input line (AI16) is reserved for reading the 6.4 volt zener voltage which is derived from the 10 volt reference.

The test consists of reading the voltage in the software, after conversion to digital by the A/D/A converter. If the voltage is in the range 6.4 ± 0.64 volts, the test passes, otherwise the test fails. If this test fails all three times it is executed as part of the 081 self test, the AO scale factor fault is set in the BIT matrix.

2. A.O. Gross Test (Word 2, Bit 4) — For this test the six analog outputs, numbered 0-6 are set to +5 volts. These digital outputs from the software are converted to analog through the A/D/A converter. The six lines are then logically combined, and the smallest voltage connected to a dedicated analog input line (AI 18). In this case all voltages are the same, so that AI 18 should have 5 volts. The voltage on AI 18 is converted back to digital through the A/D/A converter and read by the BIT software. If this voltage is 5 ± 1.5 volts the test passes. If this is the only test that fails, no faults are recorded in the BIT matrix. If this test and the AO4 individual tests fail immediately after this test, an AO Gross Fault is recorded in the BIT matrix.

3. A.O. Individual Test (Word 2, Bit 4) — For this test, AO's 2, 3, 4 are tested individually with all the other five AOs set to zero. To start all AOs are set to zero, and AO4 is set to -5 volts. This digital output from the software is converted to analog through the A/D/A converter. The six AO lines are then logically combined, and the lowest voltage put on AI 18. This result is converted to digital through the A/D/A converter, and read by the BIT software. If the result is -4.25 ± 0.85 volts, the test passes. This test for AO4 is executed three times in succession. If all three fail, the AO Gross Fault is reloaded in the BIT matrix. The entire sequence is then repeated with AO3 and AO2.

   Note that the AO for this test is -5 volts, while the input value is -4.25 volts. The 0.75 volt difference is due to a voltage drop incurred when logically combining the 6 AO lines.

4. A/D/A Linearity Test (Word 2, Bit 6) — This test uses the circuitry which permanently connects AO2 to AI 15. The BIT software outputs a sequence of voltages from -9.5 volts to 9.5 volts in 0.5 volt steps, the AO2 voltage is converted to analog through the A/D/A converter, picked up on AI 15, and converted back to digital. Through the A/D/A converter. If the voltage read on AI 15 is within ±0.2 volts at each 0.5 volt step, the test passes. If the test fails on three successive steps, an A/D/A linearity fault is set in the BIT matrix.

2.2.6 Checksum Test (Word 2, Bit 10)

The objective of this test is to detect alterations of the non-variable memory in the data processor (081). This test is performed as a time filler task in BIT continuous monitor and also as part of the 081 self test.

The checksum test sums the contents of the non-variable memory. When this computation is completed, the sum is compared to the stored value which resides in non-variable memory. The checksum value is stored at the time the 081 unit is loaded with the program.

Time Filler Checksum

The checksum task has been assigned to the lowest priority of any task executed in the tactical program. As such, the program computes checksum when it has nothing else to do. This occurs whenever the program has completed all its tasks, and is waiting for an interrupt. When executed as a time filler task, the program retrieves a pointer and a partial sum from variable memory, updates the pointer, adds the next two words flagged by the pointer to the partial sum, and stores the new pointer and partial sum. This process is repeated until all words have been added; when completed, the comparison is made, and if the computed sum is not equal to the stored value, the test fails. Three successive failures of this test will result in a radar NoGo indication. Failure of the time-filler checksum will appear in the continuous monitor BIT matrix.

081 Self Test Checksum

In addition to the checksum described above, the 081 self test computes a checksum of the read only memory (ROM) which contains utility functions such as square root, sin, cos, arctangent, etc. This checksum is compared to a constant "ROMCKSUM" which is stored in non-variable memory.

When the checksum test is executed as part of the 081 self test, it is performed un-interrupted. The execution time of the complete checksum when performed un-interrupted is about 150 milliseconds.

Three successive failures of the main checksum or three successive failures of the ROM checksum will result in a radar NoGo indication. Both checksums are each performed three times as part of each execution of the 081 self test. The 081 self test is executed:

1. At power up
2. When recovering from a power transient of sufficient duration to cause loss of transmitter time out

3. During airborne or ground initiated BIT when the power control switch on the radar set control is in the operate position.

If the test fails in initiated BIT, the initiated BIT matrix is set, otherwise the continuous monitor matrix is set. In either case, radar NoGo is sent to the BIT Control Panel.

Whenever the checksum failure occurs in either continuous monitor or Initiated BIT, an 081 failure is automatically set in the BIT matrix. This will result in setting the 081 fault indicator.

It might be noted that the checksum stored in the BIT matrix is always the correct checksum. This correct checksum is used as an identifier to indicate which version of the program has been loaded into the 081. Therefore, in the event a checksum failure, the erroneous computed value is not provided.

2.2.7 Watchdog Interrupt Test (Word 2, Bit 11)

This test detects watchdog interrupts in the data processor (081). The watchdog interrupt is an indication of an extended period (normally set by the software to about 58 milliseconds) of un-interrupted and presumably uncontrolled computing.

The 081 is equipped with an interval timer which uses a 24 bit register to count pulses of a 125 KHz clock.

Under normal circumstances, the interval timer is serviced every process sync period. This means that during every process sync period, the number of clock pulse counts in the interval timer is reduced to some value which will result in an interval timer overflow at some desired future time. The term interval timer overflow is synonymous with the term real time clock interrupt. If the time set for the interval timer overflow is later than the time of the next process sync interrupt, as long as process sync occurs regularly, the interval timer overflow will not occur.

If for some reason, either due to a hardware failure, or software error, the process sync is inhibited, the interval timer will overflow. When the interval timer overflows, the 081 watchdog logic is enabled. This logic clears the interval timer to zero clock pulse counts, and arms the watchdog overflow. From this time on, if 2^{12} clock pulses occur without a servicing

of the interval timer, a watchdog overflow will occur. The 2^{12} clock pulses corresponds to 32.768 milliseconds.

A watchdog time overflow results in a watchdog interrupt. If three watchdog interrupts occur, the failure is recorded in the BIT matrix, and a 081 fault is set. The three failure counter is cleared (set to zero) whenever Initiated BIT is run.

2.2.8 Discrete Output (D.O.) Test (Word 3, Bits 0-11)

The discrete outputs are bi-level outputs from the data processor (081) to the other components in the radar. There are 72 discrete output channels on 081 units S/N 39 and below, and 60 discrete output channels on 081 units S/N 40 and up. The discrete outputs are divided into groups of 12, so that the early model data processors have six groups, while the later models have five groups. The grouping of the discrete output channels have no particular significance. They are divided into groups of 12 so that they may be treated as bits in a half word by the software. A list of the discrete outputs is presented in Table 2.3.

The D.O. Test is executed as a part of the 081 self test. The 081 self test is performed during initiated BIT, at power up, and when recovering from a long transient. The D.O. Test is executed three times on every execution of the 081 self test. A failure is recorded in the BIT matrix only if all three attempts fail. Should the D.O. test fail three times, a radar NoGo is set, and a 081 fault is recorded in the BIT matrix. The 081 fault will eventually result in setting the 081 fault indicator.

The circuit for the D.O. Test consists of a logical OR of the twelve discrete output channels in any group. The result of this logical operation is read on a dedicated discrete input for that group.

The test is comprised of two parts, a gross test and an individual test. The gross test consists of resetting (logical 0) all twelve discrete outputs in any group. The discrete input for that group which is the logical OR of what should be 12 logical zeroes is then read. If the discrete input is not a logical zero, the test fails. Three successive failures of the test in any group will result in a radar NoGo indication, and in setting that fault in the BIT matrix labelled D.O. Group X, HI. The designated HI is used to indicate that the test failed when the discrete voltage should have been high. A high discrete voltage is equivalent to a logical zero.

The D.O. individual test is designed to check the capability of setting each discrete output to a logical ONE state. Again, a logical OR of the twelve outputs in any group is checked. In this instance, however, one of the twelve outputs in the group being tested is set to a logical one state. After a 500 microsecond wait to allow the discrete output to change state, the logical OR of eleven logical zeroes and one logical ONE is checked. If the result is not a logical ONE the test fails. The 12 discrete outputs in each group are thus tested one by one until all 12 have been tested; if any one of the 12 fails, the entire group fails. Three successive failures of the D.O. Group will result in setting the D.O. Lo BIT in the matrix for the group. The term Lo indicates that the test failed when the voltage should have been low.

A table showing the discrete output groups is presented below.

2.2.9 Radar Overheat (Word 1, Bit 9)

The solid state memory 081 units are equipped with radar overheat sensors. These sensors are designed to detect two overheat conditions:

1. Cooling air temperature in excess of 166°F, or
2. No air flow.

If either of these overheat conditions is detected, an interrupt is generated in the 081 unit. When the overheat interrupt occurs, the overheat fault is set in the BIT matrix, the radar overheat fault annunciator is set and No-Go is sent to the BIT control panel.

In addition, the message "RDRHOT" will be flashed on the VSD BIT window at a rate of two times per second. If the aircraft is on the ground, the "RDRHOT" message will flash until the radar automatically shuts down. Shutdown should occur in about 10 seconds. If the aircraft is in the air, this "RDRHOT" message will continue to flash until the power switch on the radar control panel (541) has been rotated to any other position. A return of the "RDRHOT" message even after rotation of the power switch indicates that the overheat condition persists. In airborne operation no automatic shutdown of the radar will result from overheat.

TABLE 2.3. DISCRETE OUTPUT GROUPS

081 Unit Serial Number 39 and Below

D.O. Group 0		Receiving Unit
BIT RCVR Unblanking		Receiver
BIT GTWT Drive Disable		Exciter
Spare		
Spare		
Spare		
Beacon Channel Select		Analog Signal Proc.
Spare		
Spare		
Radar Antenna Turnaround	(Not Tested)	Radar Warning Receiver
Range Rate Track	(Not Tested)	Almament Control Set
Radar On	(Not Tested)	Almament Control Set
Radar Track	(Not Tested)	Lead Computing Gyro
D.O. Group 1		
BIT Exciter Fault Set		Exciter
BIT XMTR Fault Set		Transmitter
BIT RCVR Fault Set		Receiver
BIT Antenna Fault Set		Antenna
BIT ARSP Fault Set		Analog Processor
BIT DRSP Fault Set		Digital Processor
BIT RSC Fault Set		Data Processor
BIT LVPS Fault Set		Low Voltage Power Supply
BIT RDP Fault Reset		Data Processor
BIT System Fault Set		Data Processor
BIT ANT, RSC & SYS FLT Reset		Data Processor
BIT Exciter RCVR, XMTN Fault Reset		Exciter, Receiver, Transmitter

(Continued Next Page)

(Table 2.3, Continued)

D.O. Group 2		Receiving Unit
BIT 039, 041 Fault Reset		Analog & Digital Processor
BIT Fault Reset		Low Voltage Power Supply
Spare		
Freq Band Ident BIT 1		Radar Set Control
Freq Band Ident BIT 0		Radar Set Control
BIT 610 Fault Reset		Low Voltage Power Supply
Spare		
Spare		
Spare, (Azimuth Gate)	(Not Tested)	Target Generator
Spare	(Not Tested)	
BIT Acknowledge	(Not Tested)	BIT Control Panel
Spare	(Not Tested)	
D.O. Group 3		
Spare		
Null Horn		Antenna
CWI on CMD		Transmitter
SNIFF CMD		Transmitter
Flood Antenna		Transmitter
AIM-7F PD Mode Enable		Transmitter
AIM-7F CWI Mod Enable		Exciter
CWI Drive Disable		Exciter
AIM-7F PD Mod Enable		Exciter
BIT Dummy Load Select		Transmitter
CWI On		Armament Control Set
PDI On		Armament Control Set
D.O. Group 4		
Beacon Mode		Transmitter
Beacon Mode		Receiver
Operate CMD		Transmitter

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(Table 2.3, Continued)

D.O. Group 4 (Cont.)	Receiving Unit
Chan Select BIT 2	Exciter
Chan Select BIT 1	Exciter
Chan Select BIT 0	Exciter
BIT Dummy Load Override	Transmitter
Search/Track	Receiver
Paramp IN/OUT	Receiver
ANT Hydraulics Enable	Antenna
ANT Power Enable	Low Voltage Power Supply
Channel Balance Start	Receiver
D.O. Group 5	
Spare	
Spare	
BIT RCVR TGT CMD	Transmitter
BIT ANT TGT CMD	Transmitter
BIT Fault Isolation Test	Low Voltage Power Supply
AZ Gyro	Low Voltage Power Supply
EL Gyro	Low Voltage Power Supply
Roll Gyro	Low Voltage Power Supply
Low Rate	Low Voltage Power Supply
610 Reset	Low Voltage Power Supply
Spare	
Radar Power Off	Data Processor
081 Unit Serial Number 40 and Up	
D.O. Group 0	
BIT RCVR Unblanking	Receiver
BIT GTWT Drive Disable	Exciter
039 & 041 FAULT IND Reset	Digital & Analog Signal Processor
610 FAULT IND Reset	Low Voltage Power Supply

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(Table 2.3, Continued)

D.O. Group 0 (Cont.)	Receiving Unit
Spare	
Beacon Channel Select	Analog Signal Processor
Freq Band Ident BIT 1	Radar Set Control
Freq Band Ident BIT 2	Radar Set Control
Spare	
Spare	
BIT Acknowledge	BIT Control Panel
Spare	
D.O. Group 1	
BIT Exciter Fault Set	Exciter
BIT XMTR Fault Set	Transmitter
BIT RCVR Fault Set	Receiver
BIT Antenna Fault Ind Set	Antenna
BIT ARSP Fault Set	Analog Signal Processor
BIT DRSP Fault Set	Digital Signal Processor
BIT RSC Fault Ind Set	Data Processor
BIT LVPS Fault Set	Low Voltage Power Supply
BIT RDP Fault Ind Reset	Data Processor
BIT System Fault Ind Set	Data Processor
BIT ANT, RSC & SYS FLT Ind Reset	Data Processor
BIT EXC, RCVR and XMTR Fault Ind Reset	Exciter, Receiver, Transmitter
D.O. Group 2	
Radar Power Off	Data Processor
Null Horn	Antenna
CWI on Command	Transmitter
SNIFF Command	Transmitter
Flood Antenna	Transmitter
AIM-7F PD Mode Enable	Transmitter
AIM-7F Mode Enable	Exciter

(Continued Next Page)

(Table 2.3, Concluded)

D.O. Group 2 (Cont.)		Receiving Unit
CWI Drive Disable		Exciter
AIM-7F PD Mode Enable		Exciter
BIT Dummy Load Select		Transmitter
CWI On	(Not Tested)	Armament Control Set
PDI On	(Not Tested)	Armament Control Set
D.O. Group 3		
Beacon Mode		Transmitter
Beacon Mode		Receiver
Operate Command		Transmitter
CHAN Select BIT 2		Exciter
CHAN Select BIT 1		Exciter
CHAN Select BIT 0		Exciter
BIT Dummy Load Override		Transmitter
Search/Track		Receiver
Paramp IN/OUT		Receiver
Spare		
Ant. Power Enable		Low Voltage Power Supply
Channel Balance Start		Receiver
D.O. Group 4		
BIT Rcvr Tgt CMD		Transmitter
BIT Ant. Tgt CMD		Transmitter
BIT Fault Insulation Test		Low Voltage Power Supply
Az Gyro		Low Voltage Power Supply
El Gyro		Low Voltage Power Supply
Spare		
Low Rate		Low Voltage Power Supply
610 Reset		Low Voltage Power Supply
Radar Ant. Turnaround		Radar Warning Receiver
Range Rate Track		Armament Control Set
Radar ON		Armament Control Set
Radar Track		Lead Computing Gyro

2.2.10 Scratch Pad Memory Alteration (Word 1, Bit 11; Word 12, Bit 7)

The 081 units have a scratch pad memory which contains the variable data used by the software. Since this data is variable, a checksum of the scratch pad provides no information about memory alterations. Thus, it is virtually impossible to detect isolated memory alterations in the scratch pad.

One of the memory alteration failure modes of the scratch pad is an alteration of every word. This type of fault can be detected by storing constants in reserved locations of the scratch pad, and checking later to see if the constants have been retained. This is the scratch pad memory alteration test.

For this test memory locations 40_8 to 376_8 are stored with repeated 48 bit constants as shown below.

Mem Location	Constant (Octal)			
40_8	2525	2525	5252	5252
44_8	2525	2525	5252	5252
50_8	2525	2525	5252	5252
.		.		
.		.		
.		.		
374_8	2525	2525	5252	5252

The constants in these memory locations are summed, and compared to the correct value which is stored in upper memory. If the sum computed over the locations 40_8 through 376_8 in the scratch pad is the same as the number stored in upper memory, the test passes. If not, the test fails.

The scratch pad memory alteration test is executed as a part of the 081 self test. The 081 self test is executed at power up, and during initiated BIT.

If the test fails in power up, BIT matrix word 12, Bit 7 is set. No-Go is not sent to the bit control panel, and the desired constants are stored in memory locations 40_8 to 376_8. A test failure at power up will indicate a memory alteration while the radar was turned off.

If the test fails in Initiated BIT, matrix word 1, Bit 11 is set. No-Go is sent to the BIT control panel, and the desired constants are not restored in memory locations 40_8 to 376_8. Since the constants are restored at power up (if a memory alteration occurred), a failure in Initiated BIT indicates a memory alteration since power up.

This test requires about 500 microseconds.

2.2.11 Scratch Pad Energizer Failure (Word 2, Bit 9)

The scratch pad memories in the solid state 081 unit must have power supplied at all time in order to retain data. The scratch pad memories are used to hold the variable data required by the software.

The BIT matrix data contained in the scratch pad must be retained when the radar is turned off. In order to continue to supply power to the scratch pad when the radar is off, the 081 is equipped with energizers which maintain a 5 volt supply to the scratch pad. These energizers are in effect batteries, and would probably be called batteries had they cost less.

The 081 is equipped with a circuit which checks the voltage across the energizers. If the nominal 3.9 volt output drops below 2.85 volts, a 081 discrete input line is set high. The BIT software monitors this discrete input line at two second intervals in Continuous Monitor, and at 100 millisecond intervals in Initiated BIT. If the discrete is high for three successive periods, the energizer fault is set in the BIT matrix, and No-Go sent to the BIT control panel.

2.3 RADAR SIGNAL PROCESSOR TESTS

2.3.1 041 Self Test (Word 4, Bit 0)

The 041 Self Test is in reality a series of tests. In each of these tests, the 041 is commanded to a mode, targets are inserted, and results are reported to the 081 unit. The 081 check sums the relevant IDA data, and each test in the series passes only if the exact check sum is computed.

For this series of tests, the 041 is commanded to self test mode. This command has the effect of disconnecting the 039 input to the 041 unit, and

switching in instead, a special target generator circuit installed in the 041. This target generator produces digital targets, so that there should be no noise, or statistical variation in either the magnitude or phase of these targets.

A list of these tests comprising the 041 self test is shown in Table 2.1.3-1. The octal number associated with each test is the number which will appear in the BIT matrix, Word 4, Bits 6 – 11 should the test fail. It should be noted that should more than one test fail, only the last test which failed will be reported. Since these tests are executed in numerical order, the last test which failed will have the highest number.

The 041 self test is executed at power up, and during Air or Ground Operate Initiated BIT. Each execution of the 041 self test requires about six seconds. If any of the tests fail, the 041 self test will be executed two additional times. If the 041 self test fails three successive times, the 041 self test fault is set in the BIT matrix, and No-Go is sent to the BIT Control Panel; in addition the octal number of the last test which failed is recorded. Thus, if the 041 self test passes, it will take six seconds; if it fails, it will take eighteen seconds.

The following is a brief description of each test.

Test 00 – LPRF Short Pulse Track, Format B

This test provides a minimum capability test of the LPRF track mode. It includes the ability to generate signal to noise data, as well as correct I, Q data from the range bin tracking pair.

This test is executed in short format, A.K.A. Format B and Format 1. In short format signal to noise data is formed on a 1-2-5 formula, i.e., one early noise range bin, followed by two signal or target range bins, followed by five late noise range bins. Short format is used in tactical LPRF track when the target range is too short to allow five early noise range bins.

For Test 00 a twelve bin target is inserted such that it straddles the 8 (1+2+5) range bins of the signal to noise computation. The signal level in all eight bins is the same. Thus, the signal levels reported should be in the ratio 1:2:5. These values are 77, 153, 380. These exact signal and noise

TABLE 2.1.3-1. 041 SELF TEST

TEST FAIL NUMBER

OCTAL Number	Test Which Failed
00	LPRF Short Pulse Track, Format B
01	LPRF Short Pulse Track, Format A
01	LPRF Short Pulse Track
03	LPRF Long Pulse Track
04	LPRF Short Pulse Acquisition II
05	LPRF Short Pulse Acquisition I
10	LPRF Short Pulse Search
11	MPRF Short Pulse Track
12	MPRF Long Pulse Track
15	MPRF Long Pulse Search
16	MPRF Long Pulse Search (2 Seconds)
17	MPRF Long Pulse Acquisition I
20	MPRF Short Pulse Acquisition II
21	MPRF Short Pulse Acquisition II, GCL
22	MPRF Short Pulse Acquisition II, GCL
23	MPRF Short Pulse Acquisition II, GCL
24	MPRF Short Pulse Acquisition II, GCL
25	MPRF Short Pulse Acquisition II, GCL
26	MPRF Short Pulse Acquisition II, GCL
27	MPRF Short Pulse Acquisition II, MGR
31	MPRF Short Pulse Acquisition II, MGR
33	MPRF Short Pulse Acquisition II, MGR
34	MPRF Short Pulse Acquisition II, Main Saturation
35	MPRF Short Pulse Acquisition II, Guard Saturation
36	HPRF R Dot Track
41	HPRF R Dot Search
42	HPRF R Dot Acquisition I Phase 1

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(Table 2.1.3-1, Concluded)

TEST FAIL NUMBER

OCTAL Number	Test Which Failed
43	HPRF R Dot Acquisition I Phase 2
44	HPRF R Dot Acquisition I Phase 3
45	HPRF RWS Acquisition I
50	HPRF RWS Search
52	HPRF RWS Search
53	HPRF RWS Search

levels, along with the correct corresponding I,Q data must be sent by the 041 to the 081 unit; if not, Test 00 fails.

Test 01 – LPRF Short Pulse Track, Format A

This test checks essentially the same circuits of Test 00. The difference is that Test 01 is executed in long format, A.K.A, Format A and Format 0. In long format, which is the usual tracking mode, signal to noise is computed on a formula of 5-2-5; five bins of early range noise, two bins of target, and five bins of late range noise.

This test uses the same 12 bin target of Test 00, but the position of the tracking bins is shifted. The test configuration is depicted below.

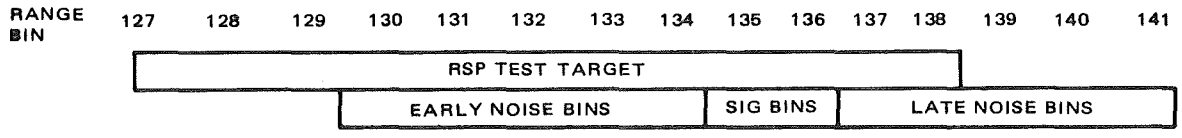

Figure 2.3.1-1 Test 01 target configuration.

As shown in the figure above, the inserted target covers the early noise bins, the signal bins, and two of the five late noise bins. Since the target level is the same in all range bins in which there is a target, the signal

levels reported for signal to noise should be in the ratio 5:2:2, for early noise, target, and late noise, respectively. The expected levels are 380, 154, 154. Together with the I,Q values from the signal bins, Test 01 passes if exactly the expected values are reported; otherwise the test fails.

Test 02 – LPRF Short Pulse Track

This test uses the same target set up and RSP mode set up as Test 01, with the exception that doppler compensation is set. Doppler compensation circuits are installed in the 041 for use in long pulse LPRF and MPRF modes. The purpose of the doppler compensation circuit is to account for doppler shifts in the target returns. If the target return doppler shifts are not compensated for, a phase shift will occur over the 13 binary phase coded range bins in long pulse mode; this will result in an attenuated target return after pulse compression. Since the doppler shift of the target return is a function of target speed, it is not possible to predict the doppler shift of the target return. It is, therefore, not possible to determine before detecting the target, the amount of doppler shift to compensate for in order to maximize probability of detection. This dilemma has been resolved by assigning fixed, but alternating, doppler compensations. The fixed doppler compensation is $\pm 22\frac{1}{2}^{o}$ of phase rotation every four range bins; thus for one microsecond range bins, the doppler compensation is about ±15.6 KHz. For the one microsecond range bins then, the doppler compensation is "tuned" alternately for 15.6 KHz opening targets, and 15.6 KHz closing targets.

The addition of doppler compensation to the target set up has a large impact on the I,Q values of the return, since the phase of return has been changed by $22\frac{1}{2}^{o}$. If this $22\frac{1}{2}^{o}$ phase change is detected, Test 02 passes, otherwise, it fails.

Test 03 – LPRF Long Pulse Track

This test exercises the pulse compression circuit.

A 13 range bin binary phase coded target is inserted so that it compresses to a single target at range bin 186. The long track format (5-2-5) is selected. The early noise range bins are 181-185, the track range bins are 186-187, and the late noise bins are 188-192. After a wait of one process

sync period, the IDA data is collected and compared against expected results. If the I,Q data and the signal to noise data are not in agreement with expected, the test fails.

Test 04 – LPRF Short Pulse Acq II

The objective of Test 04 is to verify the capability of 041 to recognize a target in LPRF Acq II mode.

The 041 is commanded to LPRF Acq II, Short Pulse, and 8X range scale. A large target, one range bin wide, is inserted so that it repeats every 45 range bins (c. 7.3 mi.). A smaller target, three range bins wide is inserted so that it repeats every 8 range bins; these smaller targets are inserted to simulate a background noise level. The presence of this background noise level will prevent false alarms when targets are thresholded.

The coarse range A is set to range bin 383 (c. 62.2 mi.), which will exclude the first 8 of the larger targets. The ninth target, at range bin 405 (c. 65.6 mi.), is detected, and range bin hit corresponding to that position is reported to the 081. If the hit is in exactly the correct range bin, the test passes; otherwise it fails.

Test 05 – LPRF Short Pulse Acq I

This test checks the ability of the 041 to detect a target in LPRF Acq I mode. As a part of this test, the post detection integration (PDI) circuits of the 041 are tested.

The 041 unit is commanded to LPRF Acq I mode, and is set to the 1X range scale. In the 1X range scale, the 041 uses a 9 to 1 PDI. A 9 to 1 PDI means that the signal from any range bin in a pulse repetition interval (PRI) is added to the signal from the corresponding range bin in the next PRI for nine successive PRIs. The result is an integration of the signals from 9 pulses, which is delivered to the 081 as IDA data.

The targets inserted for this test are the same ones used in Test 04, i.e., a large target, one bin wide which repeats every 45 range bins, and a smaller target three bins wide which repeats every 8 range bins. The smaller target is used to simulate a background noise level so that the 041 thresholding circuits will not false alarm.

The two targets are spaced such that the first large target (which appears every 45 range bins), is inserted in a gap between the small targets (which are spaced every 8 range bins). The second large target adds to one of the small targets.

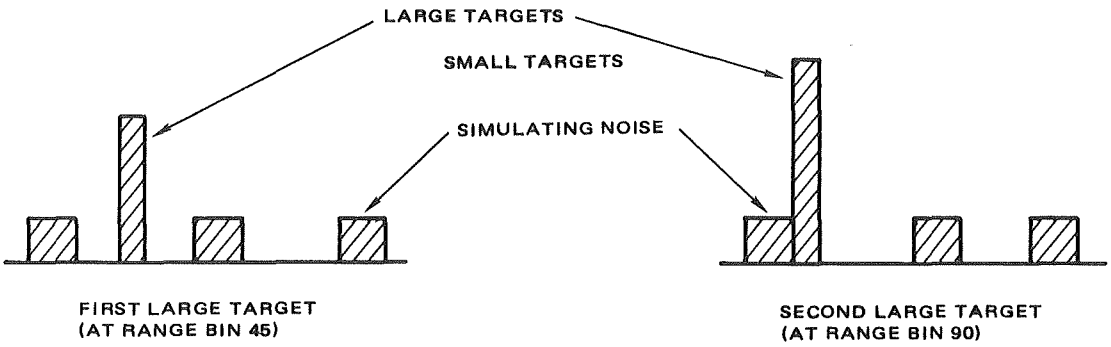

Figure 2.3.1-2. Test 05 target configuration (before PDI).

The large and small targets are not inserted in every PRI of the 9 to 1 PDI interval. Instead, the targets are timed so that after PDI, the first large target appears no larger than simulated noise level of the second target. The second large target, however, adds to the noise, so that after PDI, it appears well above the noise. Thus, the second large target should be detected, and the first large target should not be detected

Figure 2.3.1-3. Test 05 target configuration (after PDI).

The coarse Range A is set short of the first target, at range bin 31, and the 041 should report the first hit beyond coarse range A as the second large target. Any other hit results in a failure of this test.

Test 10 – LPRF Short Pulse Search

This test checks the hit counting circuits in the 041 used in LPRF search mode. In LPRF search mode, the only 041 data required by the 081 is the main channel and guard channel hit counts which are used in threshold computations.

For this test, the same two targets used in tests 04 and 05 are inserted. Then 041 then reports the main channel hits (100) and guard channel hits (0). If the exact numbers of hits are not reported, Test 10 fails.

Test 11 – MPRF Short Pulse Track Test

The objective of Test 11 is to do a minimum capability check of the MPRF track mode. This includes the ability to develop correct I,Q data from the range bin tracking pair and the filter tracking pair; it also includes a check of the ability to compute signal to noise parameters.

For Test 11, a single target is inserted which is 12 range bins long. The 041 is commanded to MPRF short pulse track, and the coarse range is set so that the target spans the tracking range bins, as well as the early and late noise range bins. The test then consists of verifying that the 041 is sending the correct I,Q data, and correct signal to noise data for the target provided. If the data is correct the test passes, otherwise it fails.

Test 12 – MPRF Long Pulse Track Test

Having completed the short pulse test, this test exercises the ability of the 041 to properly compress a long pulse target return.

For Test 12 a 13 bin binary phase coded target is inserted which should provide a compressed target at range bin 37. The 041 is commanded to MPRF long pulse track. The test then consists of checking the I,Q data to establish that the pulse compression was accomplished correctly.

Test 15 and 16 – MPRF Search

This test verifies the ability of the 041 to process targets in MPRF search, long pulse mode. Specifically, it checks the pulse compression, clutter canceller, hit counter and range resolver circuits.

For this test three targets are inserted in range bins 18, 26 and 34. All targets are in the clear region filters, so that they are visible in all nine search PRFs. The spacing of the targets in the range bins is such that they resolve to the fifth range ambiguity (range bin 290). These targets should resolve to ranges of 23.5, 30.5 and 35.6 miles.

Test 15 counts main channel hits and range resolved hits for 10 process sync periods (c. 100 ms.). After this time, the BIT software check sums the IDA data to verify that exactly the correct number of main channel hits, and range resolved hits, are reported. These should be 19 range resolved hits, and 111 main channel hits. There should be no guard channel hits. Any other totals will result in failure of Test 15.

Test 16 continues to count hits with the same targets inserted until a period of about two seconds has elapsed. By this time the range resolved hit counter should have saturated at 255. The main hit counter reads 3023, and the guard channel hit counter reads 0. If these totals are not received, the test fails.

Test 17 – MPRF Long Pulse Acq I Test

This test checks essentially the same circuits of tests 15 and 16. The primary addition is the test of the ability of the 041 to go to the MPRF Acq I state.

For Test 17 the target is moved out two bins from Test 15 to range bin 292. The first target is then at 23.6 miles. The coarse range is set inside the first target. After a four process sync wait, the BIT software checks to see if the 23.6 mile hit is reported. If so, the test passes, otherwise it fails.

Test 20 – MPRF Acquisition II, Short Pulse

Test 20 has two objectives. The primary objective is to test the ability of the 041 to recognize a target hit in MPRF Acquisition II mode. The secondary objective is to set the 041 up for the automatic gain control test 21 – 26 which follow. A description of the secondary test objective is presented in the following section.

For this test, a one bin target at range bin 34 is inserted during the second of three array periods in MPRF Acq II. During the third array period, a seven bin wide target centered in range bin 34 is inserted. Thus, when the data from the two arrays are integrated and thresholded the result should be a single target at range bin 34. The seven bin wide target inserted during the third array period is used to provide a background noise level for the threshold multiplier circuits. Without some background noise level, the threshold multipliers would operate on virtually nothing; a situation which could result in false alarms.

Both of the seven and one bin wide targets are inserted in filter number 7, and the coarse range is set to range bin 31. In MPRF Acq II, the 041 reports to the 081 any hits detected after integration and thresholding in a window seven range bins wide (beginning with the coarse range) and eleven filters wide (the center 11 of 16 MPRF filters). The target insertion pattern in Test 20 is such that the 7 X 11 hit/miss data reported to the BIT software should show hits in filters 6, 7 and 8, in range bin 34. If this hit/miss pattern is seen, the test passes. Any other hit/miss pattern results in a failure of Test 20.

Test 21 – 26 – Receiver Gain Control Level Tests

Tests 21 through 26 check the 041 gain control logic. The objective of the 041 gain control logic is to control the maximum magnitude of signal output from the 039 A/D converter. It is desireable to adjust the 039 A/D converter output so that the target magnitudes are attenuated so as not to exceed saturation.

The 041 has two mechanisms for adjusting the 039 A/D converter output magnitude. The first mechanism is a fine control which can reduce the gain of the 039 unit by as much as 40 dB, in 64 discrete steps. This fine control, called the Digital Automatic Gain Control (DAGC), is active in all modes which use the 18.4 MHz VCO, i.e., all modes except HPRF track. If the signal magnitude from the 039 A/D converter exceeds saturation even after the 039 gain has been reduced by the maximum 40 dB of DAGC, the 041 uses the second control mechanism.

The second mechanism for adjusting the 039 A/D converter output magnitude is a slower coarse control which can reduce the gain of the receiver (022) by as much as 44 dB, in four discrete 11 dB steps. This mechanism is active in all 041 modes.

It is this second mechanism, control of 022 gain, which is monitored in these tests 21 through 26. For these tests, the system remains in MPRF Acquisition II short pulse mode, as in Test 20. Test 20 was executed with the receiver gain control level at 0 dB, or no reduction in receiver gain. The test set up for Test 20 inserts a maximum sized 2-Bin target from the 041 read-only memory (BIT Target Generator) which appears to exceed 039 A/D converter saturation. The target is inserted during the pause array, thus exercising the gain control circuits.

The first test (number 21) simply waits two process sync periods to allow the 041 automatic gain control circuits to sense the over saturation condition, and then to attenuate the 022 gain by 11 dB. When the 041 commands the 11 dB attenuation, it informs the BIT software through IDA that it has done so. The test passes if the receiver gain control level is -11 dB; otherwise it fails.

The second test (number 22) waits another two process sync periods with exactly the same test set-up. Since the digital target is exactly the same, it still appears to exceed 039 A/D converter saturation. The 041 automatic gain control circuits should then command an additional 11 dB attenuation, so that the 022 gain control level is now -22 dB. The BIT software then monitors the 041 data, and will pass the test if and only if the commanded gain control level is -22 dB.

Test 23 waits four process sync periods, by which time the receiver gain control should reach the maximum 44 dB attenuation. Again passing the test can result if and only if the gain control level is -44 dB.

By this point, the gain control capability of the 041 has reached its maximum. The next test sequence removes the digital targets and requires that the receiver gain increase. Two process sync periods after the target is removed the 022 gain control level command should go to -33 dB. Test 24 passes if and only if the 022 gain control level is commanded to -33 dB.

Still with no target, another two process sync periods should drop the command to -22 dB. Test 25 passes if and only if the 022 gain control command is -22 dB.

After an additional four process sync periods, the 022 gain control level command should be 0 dB. Test 26 passes if and only if the commanded gain control level is 0 dB.

Note that this test only checks the ability of the 041 to command the 022 gain control level. It is not a requirement of this test that the receiver respond to these commands.

Tests 27, 31, 33 — Main to Guard Ratio

The objective of these tests is to check the ability of the 041 to accept or reject targets on the basis of main to guard ratio. Before a target is recognized as a range resolved hit in search and acquisition modes, it must satisfy a main to guard ratio requirement. The signal magnitude in the main channel must be at least 12 times the signal magnitude in the guard channel. (If no guard hits are detected, this requirement is bypassed.) This criterion ensures that a target hit results from a signal received from the antenna main lobe, as opposed to side lobe.

Test 27 inserts two targets at different ranges, and different velocities. The first target is at range bin 54 and filter 4, and the second target at range bin 48, filter 12. The 041 is set up in MPRF Acquisition II, short pulse mode, and both targets are one range bin wide. The main to guard ratio for both targets is so large (c. 60) that both targets should be detected, and declared hits. The 041 should report to the BIT software range resolved hit/miss data which indicates hits in range bin 54, and in range bin 48. Test 27 passes if and only if exactly this hit/miss pattern is reported. Any other hit/miss pattern results in a failure.

In Test 31 the main to guard ratio for the first target (at range bin 54) is reduced to 1.5, so it should not be declared a hit. The second target is moved to filter 5, range bin 51; and is inserted with a main to guard ratio about 30. In this case the range resolved hit/miss data should indicate a hit only in range bin 51. Test 31 passes only if and only if this hit/miss pattern is reported.

Test 33 sets the main to guard ratio for both targets to 1.5, so neither target should be declared a hit. If any hits are detected, the test fails.

Test 34 – Main Saturation

The main channel saturation logic, active in MPRF search and acquisition, is designed to reject large amplitude returns from ground moving targets. These returns are normally within the clutter notch, but, if of sufficient amplitude, may have images in the clear region filters.

The main saturation logic checks for saturated signals (all Bits set) in the notched filters. If any filter in the clutter notch is saturated in any range bin, all targets in that range bin will be rejected for all filters. Normally this mechanism will only reject targets in the outrigger filters of the clutter notch, since the main clutter return at D.C. should be rejected by the clutter canceller before filter forming. Such large amplitude returns in the outrigger filters of the clutter notch are generally associated with ground moving targets.

For Test 34 two targets are inserted in range bin 61. One target is inserted in filter 7, and one target in filter 2 (within the clutter notch). The 041 is in MPRF Acquisition II, Short Pulse Mode. The targets are sized and thresholds set so that the target in filter 2 will saturate. If the main saturation logic is functioning correctly, both targets in range bin 61 will be rejected, even though the target in filter 7 would otherwise be detected. Test 34 passes if and only if both targets are rejected.

Test 35 – Guard Saturation

The guard chanel saturation logic, active in MPRF search and acquisition, is designed to reject the altitude line. This is done by checking for signals which saturate (three most significant bits set) the guard channel in the clear region filters. If any clear region filter is saturated in the guard channel in any range bin, all targets in that range bin will be rejected.

For Test 35 two targets are inserted in the same range bin (17) and filter (5). The system is set up in MPRF Acquisition II, short pulse modes.

One target is sized so that it would normally be detected, while the second target is sized to saturate the guard channel. The 041 should then reject both targets. If it does so, the test passes, otherwise, it fails.

Test 36 – HPRF Track

Test 36 provides a minimum capability check on the HPRF track mode. The test is designed to verify the capability of forming HPRF track filters.

A target is inserted into the center of the HPRF speed gate (at filter 18). The 041 unit develops the I,Q data, and the signal to noise data. This data is translated into the proper IDA word format and transferred to the 081. If the expected I,Q and signal to noise data is not received by the 081, the test fails.

Test 41 – HPRF Search

This test checks the capability of the 041 to form the 512 filters in HPRF search mode, and checks the integrity of the hit counter circuits. In HPRF search mode the 041 reports sub-band 1 and sub-band 2 hits using a low threshold, and sub-band 1 hits using a higher threshold. These hit counts are used in threshold computations.

After target insertion, a 7 process sync counting period is allowed. The reported hit counts must be in exact agreement with expected results, otherwise the test fails.

Test 42 – 44 – HPRF R Dot Acquisition I

This test is designed to check the ability of the 041 to detect hits in R Dot Acquisition I Mode.

For this test, a different target is inserted in each of three successive process sync periods. In Test 42, a target is inserted at filter 163. Coarse range rate A is set at 127, so that the 041 should report the first hit above filter 127. This should be 163. If this exact hit is not reported, Test 42 fails.

Test 43 inserts the target at filter 147. Test 44 inserts the target at filter 179. An incorrect hit in either case will result in failure of that test.

Test 45 – RWS Acquisition I

This test checks the 041 circuits in RWS Acq I mode. Specifically, the test checks the RWS range resolver circuits.

Three targets are inserted. They are in filters 436, 442 and 448. The targets are inserted in phases C, A, B of the RWS mode. In the range resolver circuits, these targets can only be a target hit at RWS range bin 11, corresponding to a range of 22 – 24 miles. This hit corresponds to a hit in filter 436 on Phase C, 448 on Phase B and 442 on Phase A.

A coarse range of 8 is set for this test, so that the 041 should report a hit at range bin 11. If this hit is reported, the test passes, otherwise, it fails.

Tests 50 – 53 – RWS Search

This test checks the hit counting circuits of the 041 unit in RWS Search mode. Basically for this test, targets are inserted, and hit counts are allowed to build up over a period of time. Checks are made of the hit counts at several points in this interval. In addition to the hit counting circuits, the time/ensemble average mechanisms are tested.

The 041 is commanded to RWS Search mode, and time average is selected. As in other search modes, the primary information reported to the 081 in RWS Search mode is hit count data for threshold computation.

The same three targets of test 45 are inserted. These targets are all in sub-band 2, at filters 436, 442 and 448. A hit counting period of 9 process syncs is allowed. At the end of this time there should be a raw hit count of 12 in sub-band 2, and 0 in sub-band 1. If these exact totals are not reported, Test 50 fails.

The targets are turned off at this point, so that no new target hits should be entering the data stream. Since the 041 unit was commanded to time average, however, residual hits from the prior 9 process sync periods will continue to be counted as hits for another 3 process sync periods. After this time, no further hits should be counted. A period of 21 process syncs is allowed, at which time another check is made. At this point, the raw hit counts should be 18 in sub-band 2, and 0 in sub-band 1. If these exact counts are not reported, Test 51 fails.

The targets are turned on again, and a 6 process sync period is allowed. Again the hit counts are checked. This is Test 52.

Test 53 continues the hit counting for an additional 5 process syncs, this time using ensemble average. Incorrect hit totals will result in failure of Test 53.

2.3.2 039 A/D Converter Test (Word 4, Bit 1)

This test is designed to evaluate the ability of the 039 A/D converter to faithfully convert an analog signal to digital. This is accomplished by inserting a test signal into the A/D converter, which exercises the full range of allowable input signal in amplitude (4.048 volts peak to peak) and frequency (500 KHz).

The test signal is generated within the 039 when the BIT software commands Beacon to the 039, and MPRF track to the 041. This combination of commands is never used in tactical radar operation, and in effect puts the 039 into A/D converter test mode. Generation of the test signal is accomplished by commanding the 18.4 MHz VCO to a position 98,662 Hz below 18.4 MHz. This signal at 18,301,338 Hz is mixed with the output of the 18.8 MHz oscillator (which operates at 18,801,395 Hz). The mixer output is filtered to produce the 039 A/D converter input test signal.

Figure 2.3.2-1 presents a block diagram of the circuits for the A/D converter tests. The input signal at 500,057 Hz (labelled 500 KHz) is input to the four sample and hold circuits. The data in the sample and hold circuits is sampled every 1.5 μs for the PRF selected. The selected PRF is 10416.66 Hz. The output of the A/D converter is 57 Hz because the sampling scheme results in a signal frequency which is 57 modulo PRF. Since the 47th harmonic of the PRF is 500,000 Hz, the remainder is 57 Hz.

The 57 Hz signal, now in digital form is sent to the 041 unit through the clutter canceller. As indicated in Figure 2.3.2-1, the clutter canceller characteristic is such that signals with frequency below 100 Hz will be rejected. Thus, the 57 Hz signal should be rejected, and the filter processor should indicate no signal. The test is therefore passed if no signal output is detected.

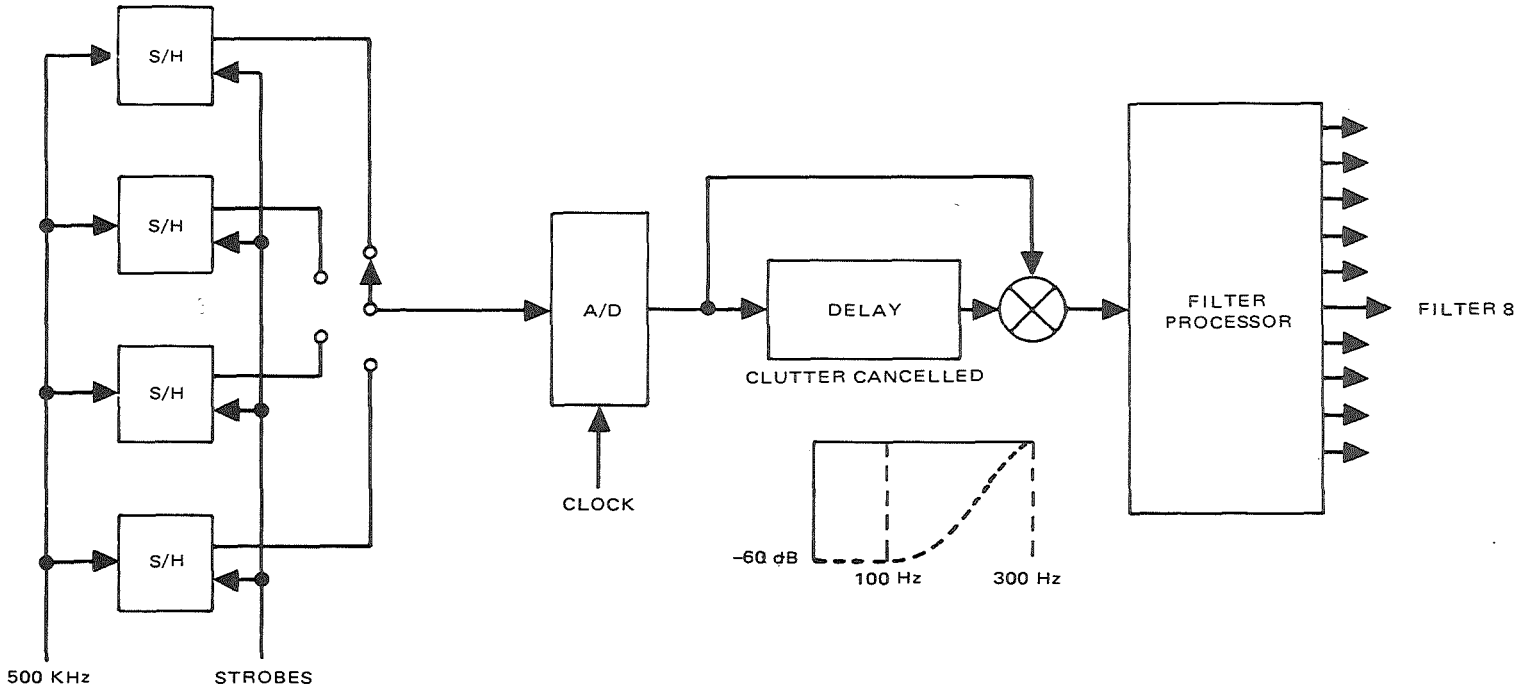

Figure 2.3.2-1. A/D converter test diagram.

Since the test consists of putting a 500 KHz signal in, and getting nothing out, the question arises, how can this test fail?

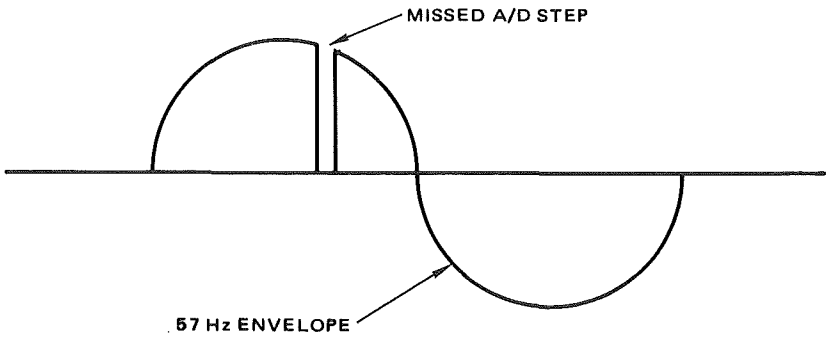

Figure 2.3.2-2. A/D converter test output for a failure condition.

The figure above shows a 57 Hz sine wave envelope with a missed step, a form of harmonic distortion. The frequency spectrum of a 57 Hz wave, without any distortion would simply be a single line at 57 Hz. With a missed step type harmonic distortion, as might be output from a faulty A/D converter, the frequency spectrum can be expected to contain a multitude of other lines at frequencies other than 57 Hz. Thus, a distorted signal will in general provide some clutter canceller and filter processor output. The presence of any such output is a good indication of signal distortion in the A/D converter.

The primary weakness of the A/D converter test described thus far is that the desired output is no signal. This could result from a perfectly operating A/D converter, or from a fault 039 which is unable to produce the 500 KHz input signal. To make sure that there is an input signal, a second part of the A/D test is executed. For this part of the test, the 18.4 MHz VCO is moved to 100,383 Hz below 18.4 MHz. This frequency produces a test signal at 501,778 Hz. The A/D converter output is then 1,778 Hz, which is well above the rejection band of the clutter canceller. For this part of the test, the 041 output is examined for signal data at 1,778 Hz, and if present, the test passes. Failure of either part constitutes a failure of the entire test.

The 039 A/D converter test is executed at power up and during initiated BIT. If the test passes, the test is executed just once. If the test fails, the

test is executed three times. A failure of the test all three times will result in a 039 A/D converter fault in the BIT matrix, a 039 fault in the BIT Matrix, and a NoGo to the BIT Control Panel.

The 039 A/D converter test is executed at the conclusion of the 041 self test. Each part of the 039 self test takes 740 ms, so that both parts use up 1.48 seconds.

2.3.3 Process Sync Interrupt Test (Word 4, Bit 2)

This test is designed to detect the loss of process sync interrupt. The process sync interrupt is the timing synchronization pulse between the digital processor (041) and the data processor (081). If the process sync interrupt is not triggered in a pre-specified period of time (normally set to about 25 milliseconds by the 081 software), the 081 will issue a real time clock overflow interrupt. If three successive real time clock interrupts occur without an intervening process sync interrupt, the process sync test fails, a radar NoGo is sent to the BIT control panel, and an 041 fault is recorded in the BIT matrix.

This test is not executed during the 041 Self Test, 081 Self Test, shutdown, power up, transient recovery, or low voltage power supply restart.

2.3.4 Interface Data Assembler (IDA) Interrupt Test (Word 4, Bit 5)

This test is designed to detect the loss of interface data assembler (IDA) interrupt. The IDA interrupt is triggered by the digital signal processor (041) to indicate that a set of radar return signal data is available for processing. In every operating mode of the F-15 radar each process sync period should have at least one IDA interrupt. If the program detects that three process sync periods have elapsed without an intervening IDA interrupt, this test fails. Failure of this test will automatically result in a 041 failure indication in the BIT matrix, in a radar NoGo to the BIT control panel, and in eventual setting of the 041 fault indicator. This test is executed only in continuous monitor.

When an IDA interrupt occurs the data processor causes the program to "interrupt" its current activity, and to begin processing the signal return data just received. Before proceeding with the interrupt processing, the 081

stores the address of next instruction to be executed (or return address) in a reserved cell; in this way when the signal return data processing has been completed, the interrupted activity can be resumed. This test uses a non-zero value of the return address to indicate that an IDA interrupt has occurred.

At each process sync interrupt* the program makes a check of the IDA interrupt return address reserved cell. If that value is not zero, an IDA interrupt is presumed to have occurred. The return address is then set to zero. If the return address is zero, no IDA interrupt has occurred, and a failure is noted. Three successive failures result in a NoGo.

2.4 EXCITER TESTS

2.4.1 Exciter Locks and L.O. Power

The exciter (001) provides three BIT discrete signals to, the Data Processor – BIT L.O. Power, BIT Offset Lock, and BIT GTWT Drive Lock. These signal outputs from the exciter are shown in Figures 2.4.1-1 and 2.4.1-2. Figure 2.4.1-1 presents the functional block diagram for 001 units serial number 126 and below, and Figure 2.4.1-2 for serial numbers 127 and up.

The BIT Offset Lock and BIT GTWT Drive Lock are discrete signals which indicate that the primary exciter outputs, the L.O. and GTWT Drive are at the proper frequency. The GTWT Drive Lock indicates that the GTWT Drive is at the proper frequency, and the offset lock indicates that the L.O. is at the correct frequency.

The L.O. power discrete indicates that L.O power is adequate.

It is noteworthy that there is no GTWT Drive Power discrete output from the exciter. It might be expected that an indication of adequate GTWT Drive Power is desired. As it turns out, there are other means of detecting low GTWT Drive Power, hence, it was decided that the additional complication incurred by adding such a signal was not justified. The most obvious

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*This test is not executed during initiated BIT, shutdown, power up, transient recovery, or low voltage power supply restart.

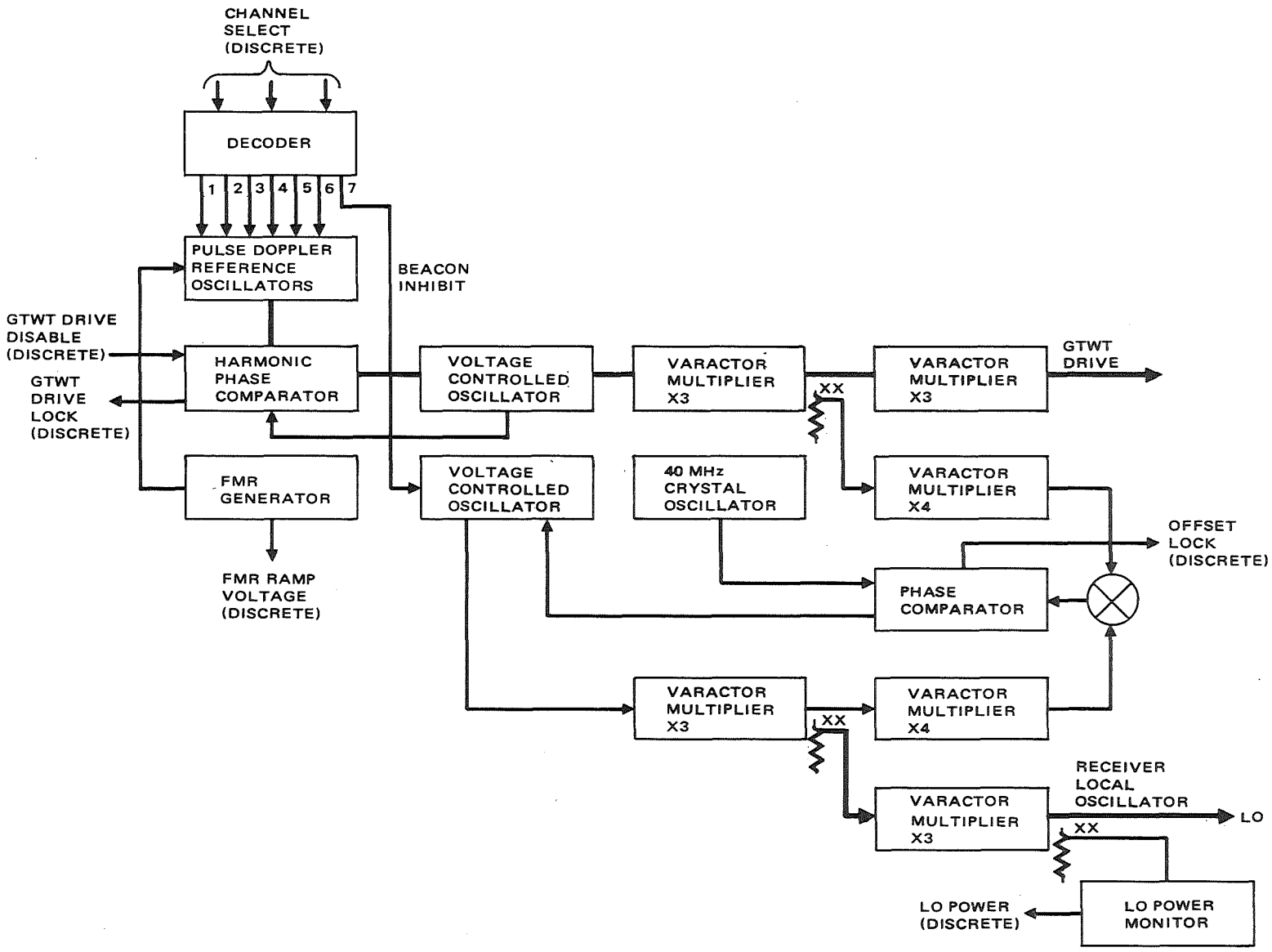

Figure 2.4.1-1. Exciter block diagram (S/N 126 & down).

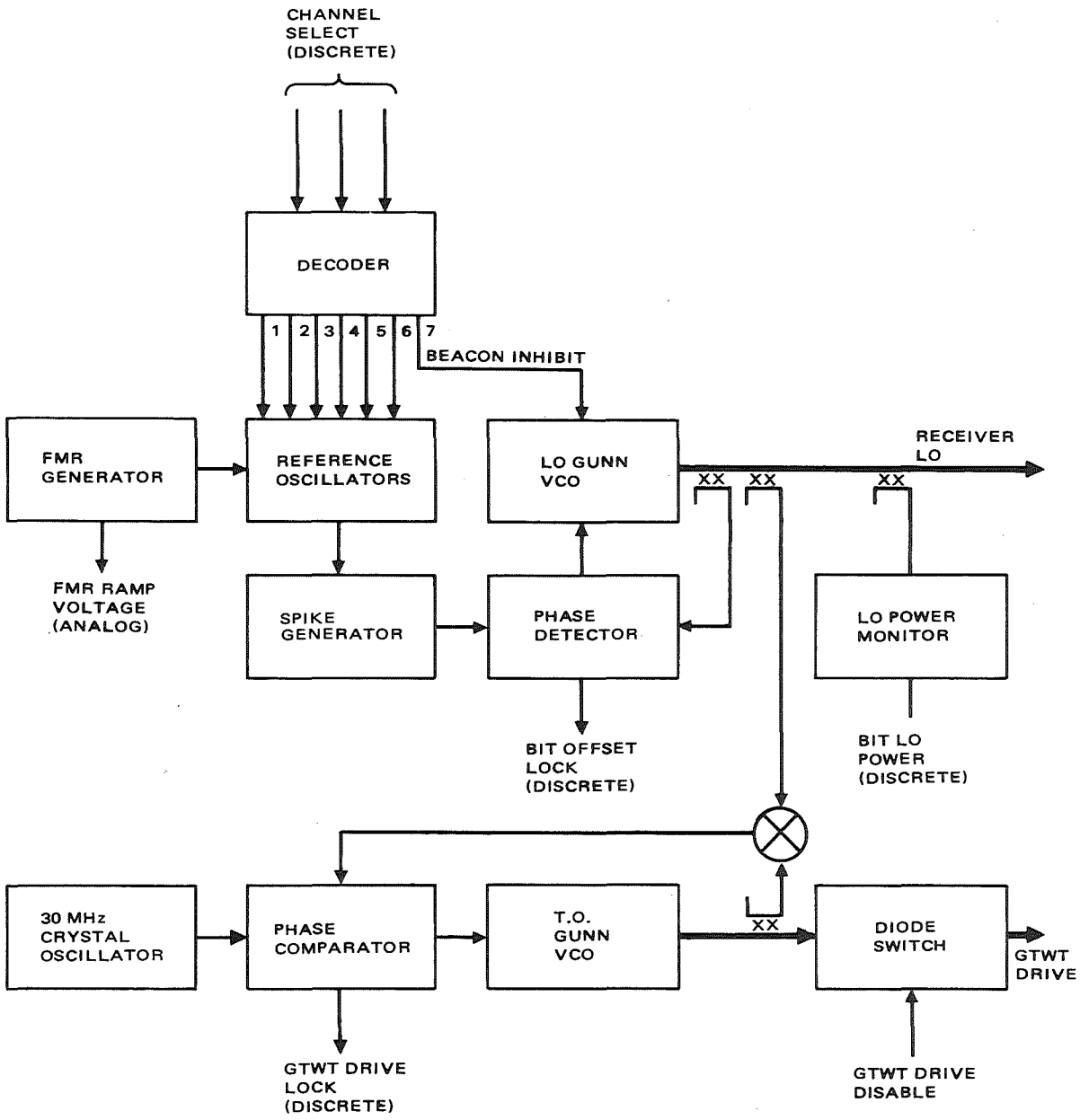

Figure 2.4.1-2. Exciter block diagram (S/N 127 & up).

means of detecting low GTWT drive power is to detect low transmitter output power. Since the GTWT amplifies the exciter drive, inadequate drive should result in inadequate transmitter output. The acquisitions tests are another check on the GTWT drive power. Since the acquisition tests use the BIT targets, and since these targets originate as the GTWT drive (see Section 2.7), inadequate drive signal should result in failure of some acquisition tests.

In the BIT software the test of exciter discretes consists of periodically checking the state of the discrete. If the discrete is in the wrong state, the test fails. Three successive failures in the same channel result in setting the bit in the matrix for that channel and sending a NoGo indication to the BIT Control Panel.

BIT L.O. Power (Word 6, Bits 0 – 5)

This output from the exciter is set to a logical one state whenever the L.O. Power Level (which is nominally 40 milliwatts) is at least 15 milliwatts. As shown in the block diagrams, this is derived by picking off the L.O. signal through a coupler, and checking power level against a threshold.

BIT GTWT Drive Lock (S/N 126 and Below) (Word 5, Bits 0 – 5)

This output from the exciter is set to a logical one state when the GTWT drive signal is locked to the reference oscillator after the frequency has been multiplied up to L band. This signal is therefore an indication that the last VCO in the GTWT drive frequency generation chain has settled. (See Figure 2.4.1-1.)

BIT Offset Lock (S/N 126 and Below) (Word 5, Bits 6 – 11)

This output from the exciter is set to a logical one state when the offset VCO has settled. This signal is an indication that the GTWT drive and L.O. signals are locked 30 MHz apart.

BIT GTWT Drive Lock (S/N 127 and Up) (Word 5, Bits 0 – 5)

This signal indicates that the L.O. Gunn VCO and the T.O. Gun VCO are locked 30 MHz apart. (See Figure 2.4.1-2.)

BIT GTWT Offset Lock (S/N 127 and Up) (Word 5, Bits 6 – 11)

This signal indicates that the L.O. Gunn VCO is locked to some known multiple of the reference oscillator frequency.

The exciter discrete tests are made periodically whenever the radar is in standby, operate or emergency, and not in beacon mode. In Initiated BIT, the tests are made nominally at 100 millisecond intervals, otherwise the tests are done at 2 second (nominal) intervals. Deviations from nominal periodicity of these tests occur as follows:

1. No exciter checks are made during a low voltage power supply re-start
2. No exciter checks are made during missile tune, or missile illumination
3. No exciter checks are made before 100 milliseconds after a channel change.

2.4.2 FMR Ramp Test (Word 6, Bit 6)

This test is designed to check the analog input voltage from the FMR Generator within the exciter (001). A block diagram of the exciter is presented in Figures 2.4.1-1 and 2.4.1-2. The FMR Generator applies a ramp voltage to the pulse doppler reference oscillator circuits. This voltage causes the oscillator to change frequency. This frequency ramp is then used in the HPRF RWS Search and Acquisition I modes to determine target range.

The FMR Generator voltage profile is shown below.

This test is executed whenever the digital process is in HPRF RWS Search or Acquisition I. Therefore in initiated BIT, this test is done during the RWS Acquisition Test, and during the RWS Power Test.

This test reads the analog voltage depicted below, and saves the largest absolute value of that voltage over 100 process sync periods.* If at the end of 100 process sync periods, the absolute value of the FMR voltage has not exceeded 2 volts, the test fails. Failure of this test results in a radar NoGo indication to the BIT control panel.

*This voltage is sampled only during Phase A,B,C. No check is made during Phase D.

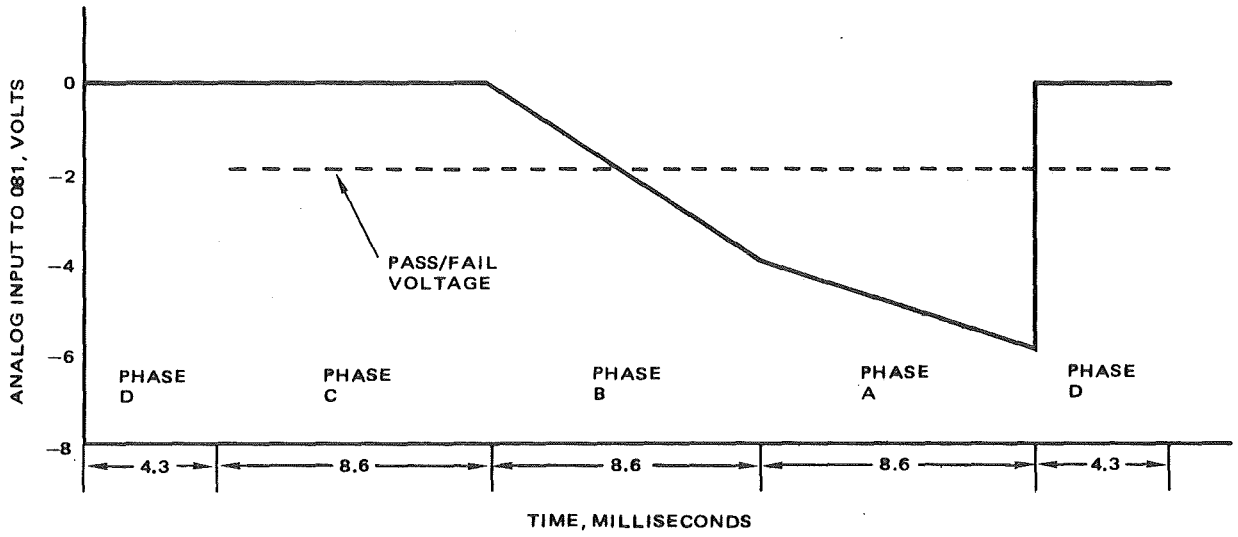

Figure 2.4.2-1. Nominal FMR voltage from exciter to data processor.

2.5 TRANSMITTER TESTS

2.5.1 RF Power Tests (Word 7, Bits 0 – 6)

The power tests detect low power output from the GTWT or from the Beacon magnetron. The transmitter is equipped with a peak power detector which is coupled to the output wave guide (see Figure 2.5.1-1). The peak power detector converts the sampled RF power into a DC voltage which is transmitted to the data processor. The data processor periodically checks the peak power detector output voltage, and compares this voltage to a pass/fail criterion. If the voltage is below the acceptable limit, the test fails. Three successive failures result in setting the appropriate RF failure in the BIT matrix, in displaying "RF NG" on the VSD, and in setting a NoGo indication to the BIT Control Panel.

The pass/fail voltage is dependent on PRF, as shown below

Mode		Minimum Acceptable Peak Power Detector Voltage
HPRF	GTWT	3.5 Volts
MPRF	GTWT	3.1 Volts
LPRF	GTWT	2.5 Volts
Beacon	Magnetron	0.75 Volts

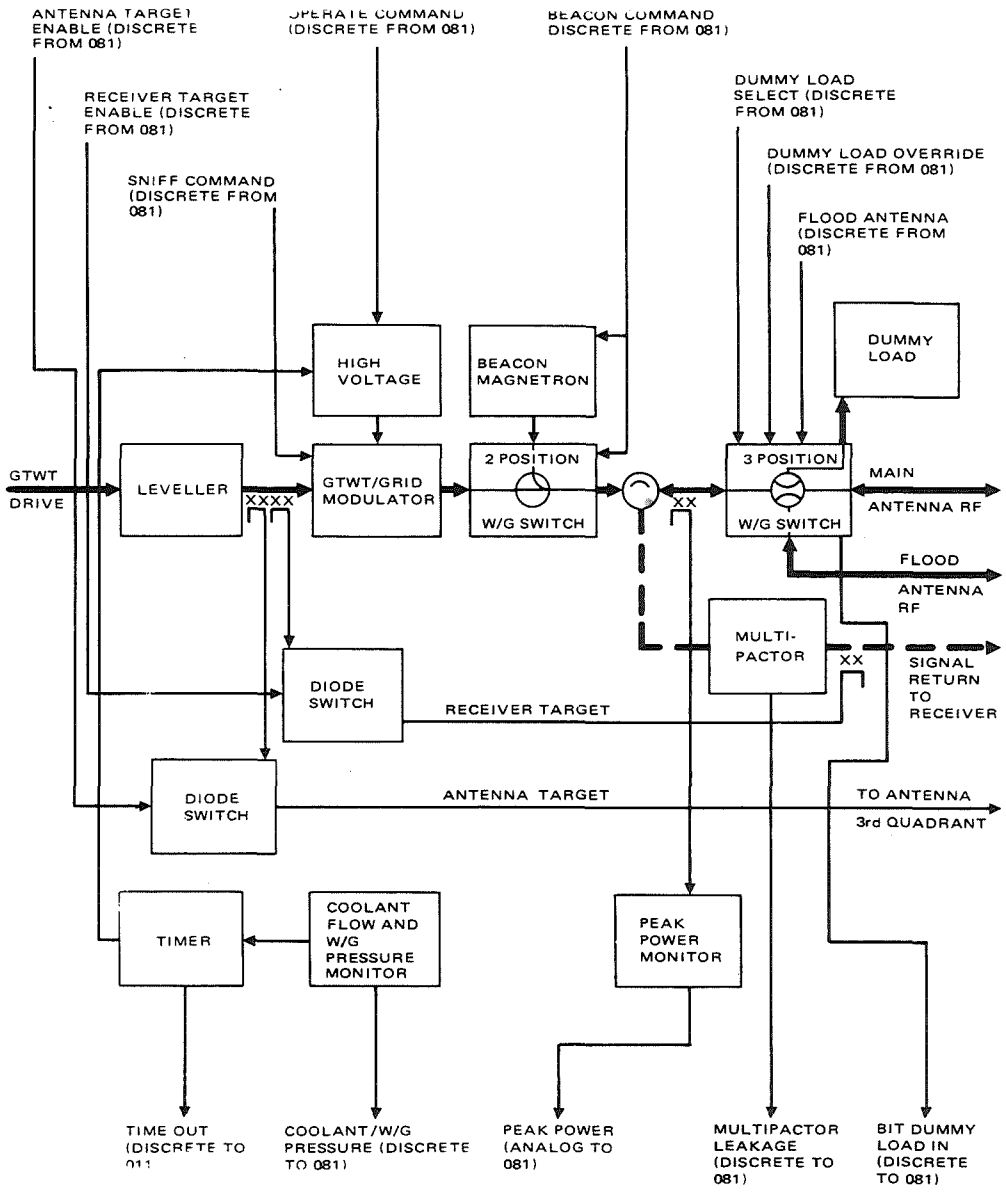

Figure 2.5.1-1. Transmitter block diagram.

It is necessary to use three different acceptance voltages for the GTWT, because both the peak power detector output and the GTWT output change with PRF. The three pass/fail voltages for the GTWT corresponds to 1360 watts at the transmitter output. This assumes one microsecond pulses in MPRF and one-half microsecond pulses in LPRF.

The RF power tests are performed both in Initiated BIT and in Continuous Monitor BIT whenever the Operate Command is sent to the transmitter or whenever the Beacon Command is sent to the transmitter except under the following conditions:

1. During a Low Voltage Power Supply Re-Start
2. During Missile Tuning or Missile Illumination
3. The First 50 Milliseconds after a Channel Change
4. Whenever Dummy Load Override is set to the transmitter
5. Whenever GTWT Drive Disable is set
6. Whenever Calibrations are in progress
7. Whenever the SNIFF Command is set and for the 10 process sync periods following the reset of the SNIFF Command
8. Whenever the GTWT drive lock fails.

Except for item 2, all power check inhibits occur when RF output is shutoff or settling. The inhibit of the missile tuning and missile illumination power checks was instituted to prevent transmitter recycle, which is described below. The RF power tests are performed at 2 second intervals in Continuous Monitor BIT, and every process sync in Initiated BIT when the above conditions are satisfied.

If the RF power test voltage falls below one volt, during Continuous Monitor BIT in Non-Beacon modes, the transmitter Operate Command is recycled. Past experience has shown that if the transmitter fails to turn on when commanded, as indicated by a less than one volt detector voltage, successful turn on can occasionally be achieved by resetting the Operate Command for some period, and trying again. The BIT software resets the operate command for one second, following failure of the one volt test, then tries again. If the transmitter fails to turn on, the Operate Command is held on for one second, then reset again for one second. After the reset period, the

Operate Command is turned on for the third time. If the transmitter still does not respond, the BIT software assumes that the problem is serious, and stops the cycling of the Operate Command. After this third try, the Operate Command is left in the ON state until a mode change or channel change is made; in either case, the three shot transmitter recycle is repeated. The transmitter recycle is inhibited in Initiated BIT. Transmitter recycle is inhibited in Continuous Monitor BIT when the transmitter self test fails. Transmitter self test failure results in setting multipactor leakage failure to the data processor. See description of multipactor fault for further information.

2.5.2 Coolant Flow Rate Low/Waveguide Pressure Low (Word 7, Bit 9)

The Transmitter (011) is equipped with a liquid coolant flow rate monitor and with a waveguide pressure monitor. If either a low flow rate of low waveguide pressure is sensed, a discrete signal is sent to the Data Processor (081).

The liquid coolant flow rate is required to be between 5.75 gpm and 3.55 gpm for proper cooling of the GTWT. The flow rate monitor will indicate satisfactory flow rate whenever the flow rate exceeds 1 gpm, and will indicate a fault whenever the flow rate drops below 0.5 gpm. Should the coolant flow rate fall below the fault level, the flow rate monitor will not only send the low flow discrete to the 081, but will also disconnect the transmitter from the aircraft AC power. Loss of AC power will result in inability to turn on the GTWT.

The waveguides are pressurized with air to between 15 psia and 19 psia. The waveguides are pressurized primarily so that any leakage will result in an out flow of air, thus reducing the probability of introduction of contaminents, such as moisture, into the waveguides. If the pressure in the waveguides falls below 10 psia, the coolant flow rate/waveguide pressure discrete signal to the 081 is set. Low waveguide pressure will not result in disabling the GTWT.

The logical OR of the low flow rate indication and the low waveguide pressure indication is sent to the 081 as discrete signal. The BIT software periodically monitors this signal. The monitoring period is two seconds in

Continuous Monitor BIT, and 100 milliseconds in Initiated BIT. If the discrete is set for three consecutive periods, a fault is set in the appropriate BIT matrix, and a No-Go is sent to the BIT Control Panel.

The coolant flow rate/waveguide pressure low discrete is also monitored during initial turn on of the radar. This activity is described in Section 2.5.3, concerning transmitter time out.

2.5.3 Transmitter Time Out (Word 7, Bit 8)

Transmitter time out is a discrete input to the Data Processor (081) from the Transmitter (011). This discrete is nominally set by the transmitter three minutes after the liquid coolant flow rate has reached a satisfactory level. Turning the radar on from the Radar Set Control (541) starts the liquid coolant pumps. The liquid coolant pumps should establish a proper coolant flow rate in 2 — 5 seconds, so that the transmitter three minute timer should start in 2 — 5 seconds after the radar is turned on.

The purpose of the three minute wait is to allow the cathode in the GTWT to warm up to a proper temperature. This protects the cathode from being boiled away, a situation which could occur if high voltage were applied to a cold cathode.

The three minute wait is a maximum, and could be less, depending on the length of time the system has been off. If off for more than a few seconds the wait time is maximum. The transmitter will not enable the high voltage until transmitter time out, thus no radiation of RF energy can occur without time out. (See Figure 2.5.1-1.)

Because past tests at low temperature have shown that the coolant flow rate sometimes takes considerably longer than the nominal 2 — 5 seconds, the software allows 5 minutes. For a period up to 5 minutes after turn on, the software monitors the coolant flow rate discrete. If the satisfactory flow rate indication is not received in 5 minutes, a coolant fault is set in the BIT matrix and NoGo is sent to the BIT Control Panel.

As soon as the satisfactory flow rate indication is received, or if 5 minutes elapses, the software begins a 3 1/2 minute timer. If the transmitter 3 minute timer does not expire in the 3 1/2 minute period the transmitter time out fault is set in the BIT matrix, the 011 fault is set, and a NoGo

indication is sent to the BIT Control Panel. During the course of the wait for transmitter time out, the coolant flow rate discrete is monitored about every 840 milliseconds. If the coolant discrete should indicate unsatisfactory flow rate for 3 successive periods, a coolant flow rate fault is set in the BIT matrix, and NoGo sent to the BIT Control Panel.

If the transmitter time out is received within the 3 1/2 minutes, the BIT software, thereafter, periodically checks the time out discrete. The test interval is 2 seconds in Continuous Monitor BIT, and 100 milliseconds in Initiated BIT. If the transmitter time out is not received for three successive periods, the time out fault, 011 fault, and NoGo are set.

In the case of loss of transmitter time out the setting of the 011 fault in the BIT matrix does not automatically result in setting the 011 fault indicator. If the transmitter coolant flow fails, a hardware interlock within the transmitter will automatically reset the transmitter time out. In this case both the transmitter time out and coolant faults will be set in the BIT matrix. Since the coolant supply is external to the transmitter, a coolant failure will result in resetting the 011 fault in the BIT matrix. The net result is that a loss of transmitter time out will result in a 011 fault, unless transmitter coolant also fails; in that case no radar unit fault will result.

2.5.4 Dummy Load Test (Word 7, Bit 10)

The Transmitter (011) is equipped with a three position waveguide switch which directs the GTWT output energy to the Main Antenna, the Flood Antenna, or to the Transmitter Dummy Load (see Figure 2.5.1-1). The waveguide switch is in the Dummy Load position whenever the aircraft nose wheel is on the ground or whenever the Dummy Load is selected by the Data Processor (081), except when Dummy Load Override is selected by the 081. When Dummy Load Override is selected, the waveguide switch is set to the Main Antenna position.

The Dummy Load is used primarily when the aircraft is on the ground as a safety feature. Radiating into the Dummy Load precludes the possibility of radiating any personnel who might be walking about in the main beam, while the aircraft is parked. The Dummy Load Override feature, by selecting

main antenna, allows returns from the BIT antenna target to reach the receiver. As an additional safety feature, the transmitter will not enable high voltage (and thus the GTWT) whenever Dummy Load Override is set.

When the waveguide switch is in the Dummy Load position, the transmitter sends a discrete to the 081 indicating that the Dummy Load is in. The BIT software monitors the Dummy Load in discrete from the transmitter every process sync period in Search, Acquisition and in Initiated BIT. The waveguide switch position is compared to the desired position for the particular mode of operation, and if not correct, logs a fault. If the waveguide switch is in the wrong position for three consecutive process sync periods, the fault is set in the BIT matrix and NO-GO is sent to the BIT Control Panel.

2.5.5 Multipactor Fault/011 Self Test Fault (Word 7, Bit 11; Word 7, Bit 7)

The transmitter (011) sends a discrete signal to the data processor called BIT Multipactor Fault. Figure 2.5.5-1 presents a diagram of the logic comprising this discrete.

The BIT Multipactor Fault is the result of the logical OR of excessive flat leakage, low coolant flow rate, and a transmitter fault which could result from a number of causes.

1. Low Coolant Flow – A low coolant flow rate fault will also result in setting of coolant flow/waveguide pressure discrete from the 011. The conditions for low coolant flow are described in Section 2.5.2. This fault will cause loss of high voltage.
2. Excessive Flat Leakage – The multipactor is designed to protect the receiver from excessive transmitter leakage power levels. It is designed to limit any return to 10 watts flat leakage, and 25 watts spike leakage.

   The BIT multipactor leakage monitor sets the excessive leakage signal whenever the leakage exceeds 15 watts. There is no BIT multipactor spike leakage test. This fault will not cause loss of high voltage.
3. Transmitter Fault – The third possible cause of setting the BIT Multipactor Fault discrete is a transmitter fault which will result in disabling the high voltage. As shown in the logic diagram, the 011 fault is the result of the logical AND of emergency not set, SNIFF not set, and the high voltage disabled fault.

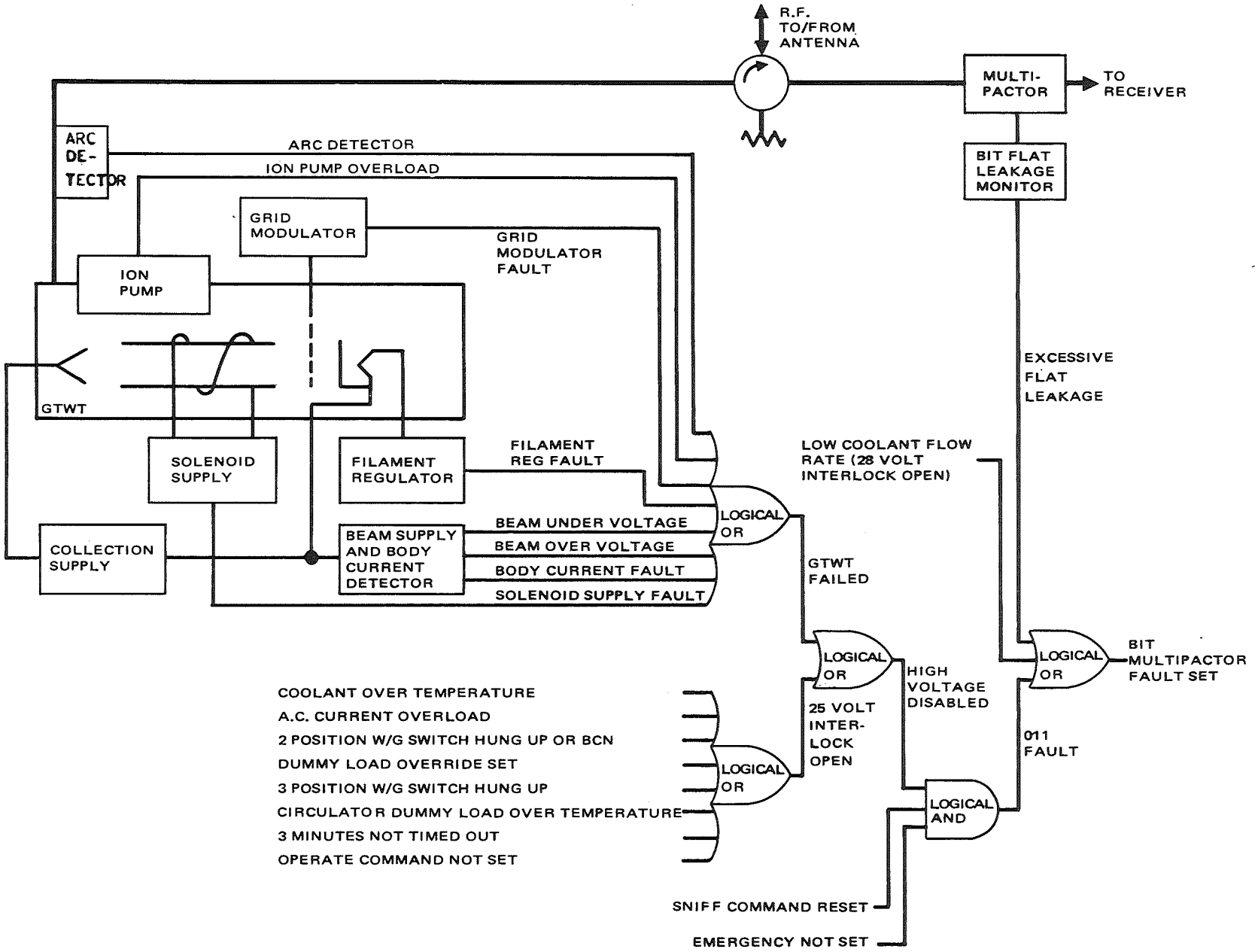

Figure 2.5.5-1. BIT multipactor fault logic diagram.

A transmitter fault which would ordinarily result in setting BIT Multipactor Fault is over-ridden when either Emergency is set on the Radar Control Panel (541), or the SNIFF command is set by the Data Processor (081). Thus, selection of Emergency or SNIFF will reset the BIT Multipactor Fault.

Assuming that the Emergency and SNIFF commands are reset, the BIT Multipactor Fault can be set by any fault which disables the high voltage. These faults are divided into two sub-groups.

25 Volt Interlock

In order to enable the high voltage, and thus generate R.F. power, the 25 volt interlock must be closed. Before this interlock can be closed, a number of checks are made:

1. Coolant over/temperature — The liquid coolant temperature is typically 145°F. If this temperature exceeds 195° ± 5°F, the 25 volt interlock will open.
2. AC Current Overload — If the transmitter draws more than 130 AMPS of 400 cycle, 115 volt power, the 25 volt interlock will open.
3. Two Position W/G Switch — If the 2 position waveguide switch is between detent positions, or in the Beacon position, the 25 volt interlock will open.
4. Dummy Load Override — If the dummy load override discrete is set by the 081, the 25 volt interlock will open. Dummy load override will set the 3 position waveguide switch to the main antenna position even if the aircraft is on the ground.
5. Three Position W/G Switch — If the 3 position waveguide switch is between detent positions, the 25 volt interlock will open. Note: CCP 565 removes this function from the 25 volt interlock line.
6. Circulator Dummy Load Temperature — The circulator which directs GTWT output to the antenna, and the return signal to the receiver has attached to it a dummy load. The purpose of this dummy load is to absorb energy reflected by the multipactor. If the temperature of this dummy load exceeds 320° ± 7°F, the 25 volt interlock will open.
7. Three Minutes Not Timed Out — The 25 volt interlock will be open until a three minute timer expires following system turn on. In the event that the timer fails to expire, a separate discrete is set by the 011. A more detailed discussion is presented in Section 2.5.3.

8. Operate Command Not Set – The 25 volt interlock is open whenever Standby is selected on the 541. This by itself would cause the BIT Multipactor Fault to be set, however, in actual practice, the SNIFF command is always set by the software when Standby is selected. The selection of SNIFF will override the 25 volt interlock.

GTWT Tests

The transmitter tests some of the GTWT protection circuits. If any of these tests fail, the high voltage is not enabled.

1. Solenoid Power – If the solenoid power supply is not on, the test fails.
2. Ion Pump – The purpose of the Ion Pump is to maintain a high vacuum in the GTWT. If the Ion pump senses a current in excess of 15 micro amps, the GTWT is assumed to be too gassey, and the test fails.
3. Arc Detected – In theory any waveguide arcs should travel back to the output window of the GTWT. The transmitter is equipped with a photo detector which will sense a R.F. arc in the GTWT window. If an arc is sensed, the test fails.
4. Body Current – If the electron beam in the GTWT spreads enough to result in a greater than 270 milliamps body current, during transmit periods, and 100 milliamps during non-transmit periods, the test fails.
5. Grid Modulator – This test checks the integrity of the grid modulator pulse on the grid (pulse amplitude, rise and fall times); and over and under voltage. If unsatisfactory, this test fails.
6. Beam Over Voltage – This nominal voltage is 12 KV. If the beam voltage exceeds 13 KV, this test fails.
7. Beam Under Voltage – If the beam voltage is below 11 KV, this test fails.
8. Filament Regulator – This test checks for an operational filament regulator.

The first six of the GTWT tests are executed continuously when the GTWT is on. The remaining two are only checked at start up. Start up occurs when the operate command is initiated. In the strictest sense tests 7 and 8 above will not result in loss of high voltage, but in loss of grid modulator trigger.

If one of the tests fail while the GTWT is on, the GTWT will shut down, and execute a self test. If the self test fails, the GTWT will not re-start. If

the self test passes, the GTWT will re-start, however, another test failure within 3 seconds will result in shut down until the operate command is re-cycled.

Any of four faults (self test, 25 volt interlock, flat leakage 28 volt interlock) can result in BIT Multipactor Fault. The BIT software in the 081 periodically monitors the multipactor fault discrete signal from the transmitter. The test periods are every 2 seconds in Continuous Monitor BIT, and every 100 milliseconds in Initiated BIT. If this discrete indicates a failure three times in a row, a failure will be set in the BIT matrix.

The type of fault set in the BIT matrix depends on whether or not the RF power test passed. If the fault is not accompanied by a RF power fault, the transmitter must have passed the 011 self test, so the multipactor fault indication from the transmitter must be a faulty multipactor. Therefore, the multipactor fault will be set in the BIT matrix.

If the fault is accompanied by a RF power fault, the transmitter never turned on, so that there could not be excessive multipactor leakage. In this case, the multipactor fault indication is interpreted as a 011 self test fault, resulting from one or more of the myriad faults described above. Therefore, the 011 self test fault will be set in the BIT matrix.

In either case of multipactor fault or 011 self fault, a NoGo indication is sent to the BIT Control Panel.

2.6 SYSTEM CALIBRATIONS

2.6.1 18.4 MHz and 22.8 MHz VCO Calibration (Word 8, Bit 0; Word 8, Bit 4)

The VCOs in the Analog Signal Processor (039) convert the receiver I-F output signals to lower frequency signals suitable for processing in the subsequent circuits. These VCOs are calibrated to compensate for any drift in the 30 MHz offset frequency existing between the receiver local oscillator and GTWT drive signal frequencies in the Exciter. If the VCOs were not compensated for the drift error, target signals at the output of the 039 would be in error.

The discrete calibration ON command to the 039 initiates the VCO calibration. The BIT Antenna Target is enabled in the HPRF mode to provide a

CW signal source derived from the GTWT drive. This signal is mixed with the receiver local oscillator signal to provide an I-F signal to the 039 of 30 MHz ± drive frequency (fe).

The 041 mode enables either the 18.4 MHz or the 22.8 MHz VCO; HPRF search enables the 18.4 MHz VCO, HPRF track enables the 22.8 MHz VCO. Calibration of the 18.4 MHz VCO is as follows: Control of the VCO is transferred from the normal input command to a fixed command signal stored in a read-only memory (ROM) device. The 30 MHz ± fe input signal is mixed with the VCO output signal in the 039. The difference signal is then processed in the normal manner to produce an output at the phase detectors. This output signal has a frequency of 15 KHz ± fe. During the calibration mode, the phase detector output signal is connected to the frequency counter. The resulting count is compared to a number stored in the ROM and the difference is stored in a read-write memory device as the offset frequency error. This stored number is then used as an error correction term to be added to the VCO input command during normal operation of the VCO. The resulting signals at the output of the 039 will then represent the true doppler frequency shifts of the received RF target signals.

The 22.8 MHz VCO is calibrated in the same manner as the 18.4 MHz VCO except that the VCO frequency is set to provide phase detector output of 2,092 Hz. The output signal is then counted and compared to a fixed number as before. The difference frequency is stored in read-write memory as the offset frequency drift and is used to correct VCO commands.

At the conclusion of each VCO calibration a verification is made. For the 18.4 MHz VCO, the system is put into HPRF VS Acq I mode. The VCO is positioned so that the antenna target appears in the middle of sub-band 1, and a check is made for the correct filter hit. The VCO is positioned to 15,712 Hz above 18.4 MHz, which should place the antenna target (which is at 0 Doppler) in filter 128. If the target is found in filter 128 ± 2 (116.2 Hz Filters), the calibration is considered successful.

The 22.8 MHz VCO calibration verification is similar except that the system is in HPRF track. The 22.8 MHz VCO is commanded to 22.8 MHz, which should place the antenna target in the middle of the speed gate at filter 18. If the target is found in filter 18 ± 1 (116.2 Hz Filter), the calibration is considered successful.

If either verification should fail to find the target in the acceptance window, a failure will be logged. If either verification fails three successive times, a failure for that VCO is marked in the BIT Matrix, and a NoGo is sent to the BIT Control Panel.

The failure margin for the VCO verification is so large that these tests cannot be used to measure system sensitivity. Even if the antenna target was attenuated 40 dB, the VCOs would still probably calibrate correctly.

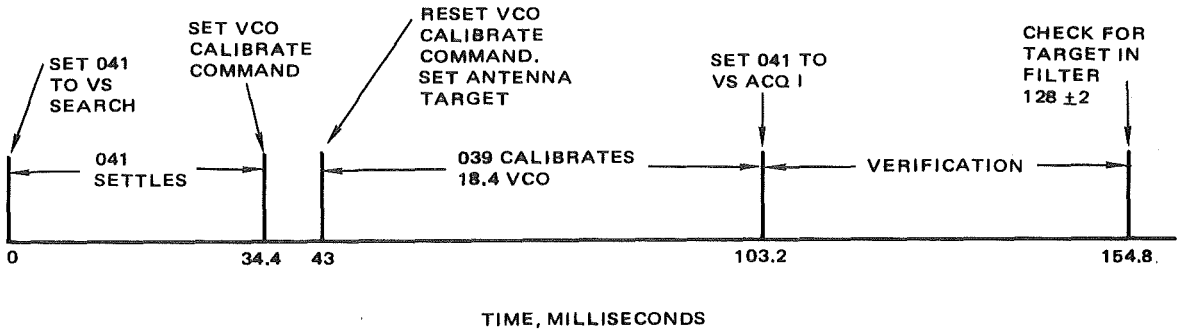

Figure 2.6.1-1. 18.4 VCO calibration time line.

The time line above indicates the various aspects of the calibration of the 18.4 MHz VCO. After an initial settling period, the VCO calibration command is sent to the 041. The 041 relays this command to the 039. After one IDA period (8.6 ms) the VCO calibrate command is reset, and the antenna target is enabled. For the following 60.2 milliseconds, the VCO calibration circuits internal to the 039 take over. After the 60.2 milliseconds have elapsed, this calibration is assumed to have been completed, and the verification is started. After 51.6 milliseconds, a pass/fail check is made.

The time line for the 22.8 MHz VCO is nearly the same as for the 18.4 MHz VCO, except that the time which the BIT software allows for the 039 internal calibration is 51.6 milliseconds, instead of 60.2; and the verification setting period is slightly longer.

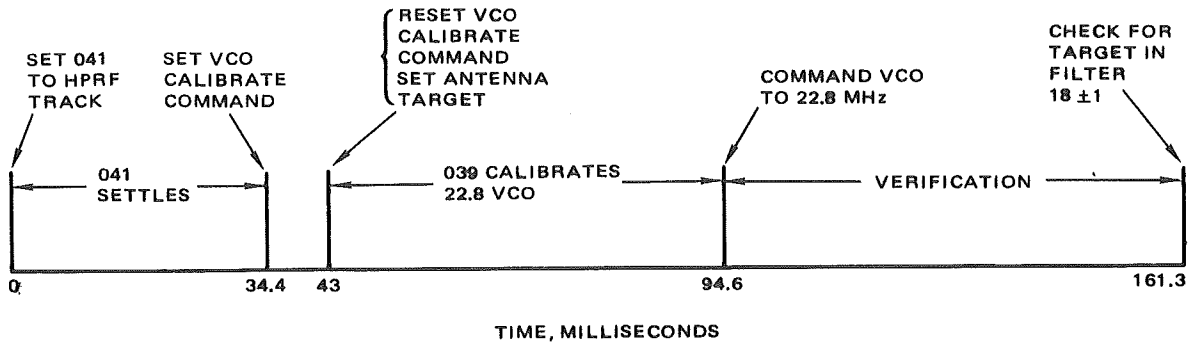

Figure 2.6.1-2. 22.8 VCO calibration time line.

2.6.2 Range Delay Calibration (Word 8, Bit 3)

The Range Delay Calibration is designed to determine the range error which results because of time delays introduced into the return signal processing. This can be understood more easily if it is imagined that the radar is tracking a target at zero range, at the antenna face. Assume that at time zero, the signal processor (041) commands the transmitter to send an infinitesimally narrow pulse. The time between the time that the transmitter is gated on, and the time that the return signal from the zero range target reaches the 041 is the time of interest for the range delay calibration. If the 041 began processing return data immediately at the time the transmitter was gated on, the time delay before the 041 sees the zero range target return would be interpreted as a non-zero range. If this apparent range is subtracted out, the result is the correct zero range. The value of the apparent range (which was subtracted out) is stored in the software as the range delay calibration. The value is expressed in units of feet.

During track, the range delay calibration is used to correct target range. No range correction is made in search or acquisition modes, since precise range is not required.

The range delay calibration is executed only in ground/operate Initiated BIT under the following conditions:

1. Transmitter timed out
2. Operate command set
3. Weight on wheels (implies aircraft is on ground)
4. Dummy load in.

When these conditions are satisfied, the Initiated BIT software will execute the range delay calibration eight (8) times, and store as the calibration value the average of these eight values. If the conditions are not satisfied, the calibration is skipped.

The range delay calibration is performed with the system in MPRF track mode. The PRF selected is the major (66 bin) of PRF Number 7 (1.6 microsecond pulses) in short pulse mode.

Under all operating conditions, the signal processor (041) controls the pulsing of the transmitter in MPRF mode. In tactical mode, the 041 will gate a pulse on, then for the 66 bin PRFs, will process data for the next 63 bin periods (the last two bins are not processed). When the 041 is in continuous monitor mode (which is the case for the range delay calibration), the pulse gate to the transmitter is delayed. For the 66 bin PRFs, the delay is 20 bins. This delay will result in generating a trasmitter pulse during what would normally be the interpulse processing period.

In the range delay calibration, since the Operate Command is set, the pulse gated 20 bins into the inter-pulse period will result in pulsing the GTWT. The RF energy output from the GTWT is then partially reflected off the dummy load, and propagates back through the signal return path as a target in range bin 20.

The signal return processing in the 041 is unaffected by 20 bin delay, and therefore, processes range bin 20 like any other range bin. Since the signal processing is beginning simultaneously with the pulse, the time that the target takes to reach the dummy load, then propagate back through the transmitter, receiver, and analog signal processor, will be interpreted as a target range beyond range bin 20.

The coarse range B is set to form a range discriminant assuming the target is exactly at range bin 20. The signal return propagation time, however, will shift the target out of range bin 20, so that it straddles range bins 20 and 21. The range discriminant will therefore indicate that the range is in error. This error is reduced by incrementing the fine range command.

The fine range command originates in the data processor (081) and is sent to the 041. The fine range command causes a delay in processing signal return data. The program may command as many as 32 steps of about 50 nanoseconds or 24.6 feet.

With the fine range set to zero, the range discriminant will indicate that the estimate of range is low, as indicated above. The fine range is then stepped up to one. This will delay signal return processing by about 50 nanoseconds, so that return processing is not begun simultaneously with the gate command to the transmitter, but 50 nanoseconds later. The range discriminant is formed again, and if the range estimate is still low, the fine range is incremented again. This process of discriminant forming and fine range incrementing is continued until the discriminant indicates that the range estimate is too high. At this point, the range estimate has been corrected to within one fine range step, or 24.6 feet.

Using the last discriminant values, the BIT software range delay calibration scheme interpolates to determine the fraction of the fine range step which would correspond to an exact range estimate. This exact range estimate will now be some integer number of fine range steps beyond range bin 20, plus an interpolated fraction. Since it is known that the target was generated at exactly range bin 20, the excess beyond range bin 20 must then be the processing delay. Expressed in feet, this is called the range delay calibration.

After the range delay calibration has been computed, the fine range is dropped back to zero, and the process is repeated 8 times. The eight values of range delay are then averaged. If any of the eight values are zero, they are excluded from the averaging. Fine range values less than four are also excluded.

The resulting average value is then compared to limits of 100 to 600 feet. If the average of the eight computations results in a value outside these limits, that value is scrapped, a failure is logged and another set of eight range delay measurements is made. If still outside the limits, another set of eight is taken.

If this third set is also outside the limits, the range delay calibration fails; a failure is recorded in the BIT matrix, a NoGo is sent to the BIT Control Panel, and a nominal value of 400 feet is stored as the range delay calibration.

It might be observed that the range delay calibration is supposed to account for processing delays from the antenna to the 041, yet the test only measures delays between the transmitter dummy load and the 041. This is justified for two reasons. First, measurements indicate that most of the delay occurs in the analog signal processor (039), so that no great error is introduced by skipping the antenna. Second, the reflected RF pulse from the antenna may be smaller, at some frequencies, than the leakage RF pulse around the four-port circulator in the transmitter, resulting in a frequency dependent range delay calibration.

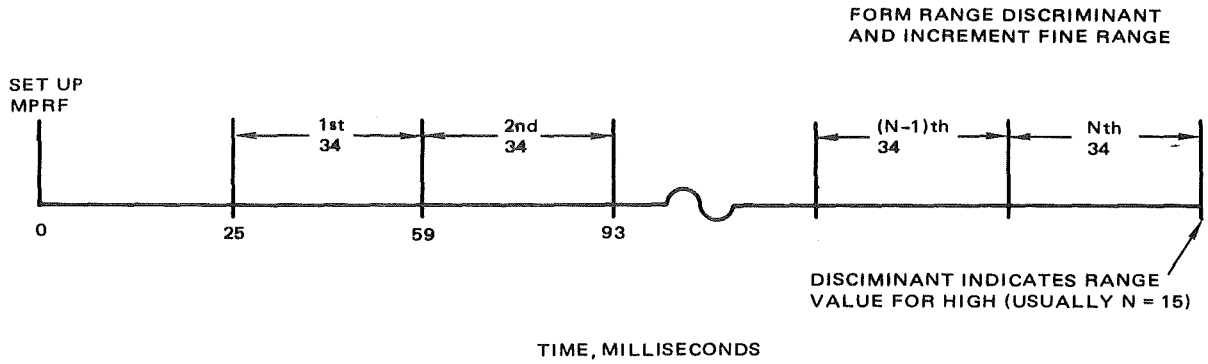

Figure 2.6.2-1. Range delay calibration time line.

The time line above presents the schedule for one of the eight computations of range delay. After a 25 millisecond set-up period, a sequence of discriminant forming and fine range increment (usually N = 15) is required. This results in a total of about 510 milliseconds required to compute one value of range delay. For a set of 8, 4.1 seconds is required.

2.6.3 Receiver Phase Balance Calibration (Word 8, Bit 1)

The Receiver (022) is equipped with a phase balance circuit as shown in Figure 2.6.3-1. The purpose of the Receiver Phase Balance Calibration

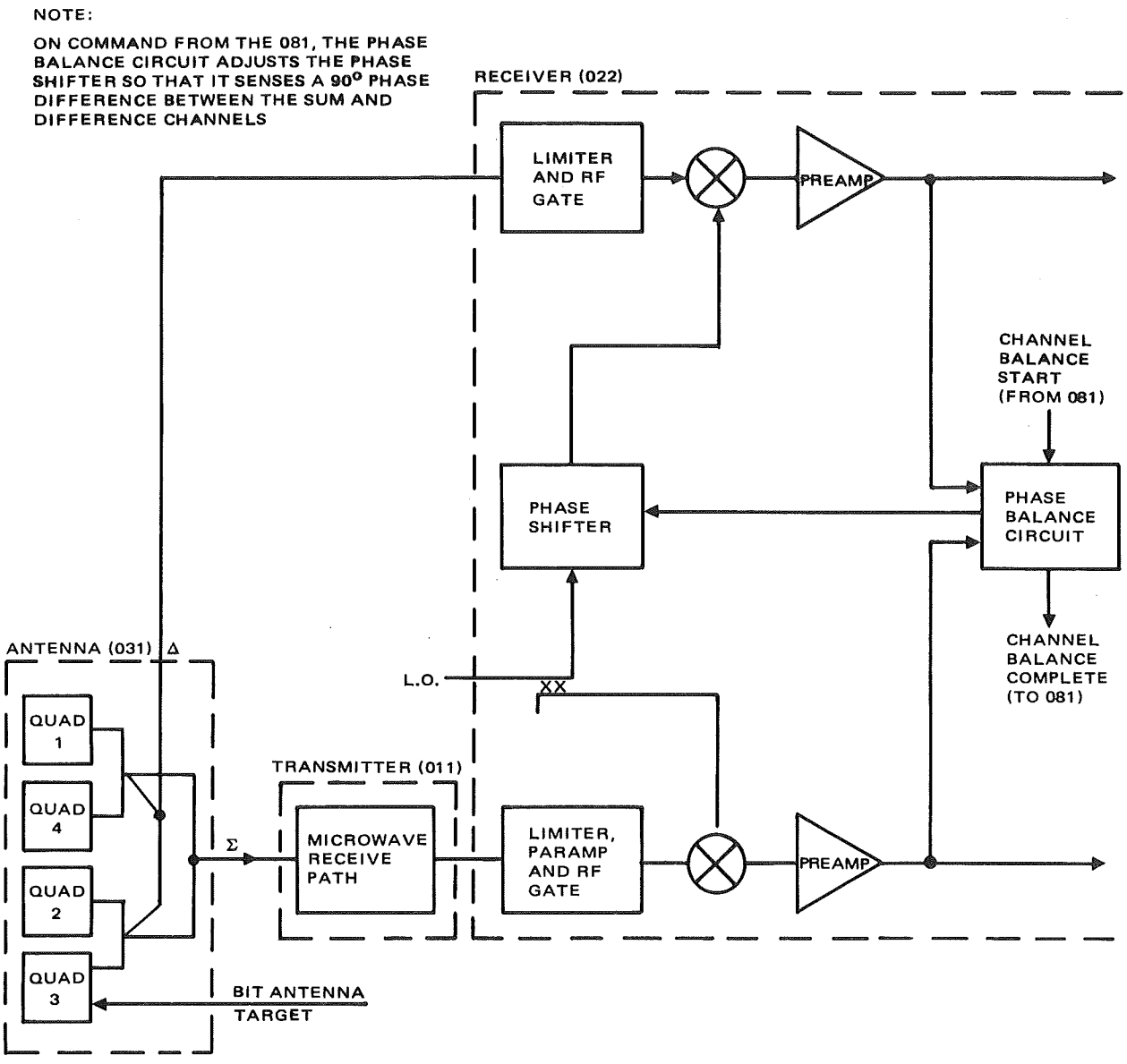

Figure 2.6.3-1. Receiver phase balance calibration.

is to compensate for any sum and difference channel phase differences which are introduced between the antenna and receiver. These phase differences could be caused by unequal lengths of waveguide, or because of the presence of filters, gates, limiters, or any other device in the signal return lines. The minimization of inter-channel phase error is required in track mode for angle tracking, and in air-to-ground ranging monopulse mode. The search, acquisition, and flood track modes do not require proper phase balance.

In the phase calibration, the BIT antenna target is inserted into one quadrant of the antenna, and the phase balance circuit is enabled on command from the data processor (081). The antenna outputs are sum and difference signals which are equal in magnitude. The phase balance circuit commands the phase shifter circuit to shift the phase of the local oscillator (L.O.) signal to the delta channel in 22 1/2° steps until the phase balance circuit senses a 90° phase difference between the two channels. Since the phase shifter steps are 22 1/2°, the resulting phase difference between channels cannot in general be exactly 90°, but only within 22 1/2° of 90°. The setting of the phase shifter which results in the closest to 90° difference is then saved, and that value is used to correct phase errors in tactical tracking conditions. The receiver then sends channel balance complete to the 081.

When the antenna target is inserted, the sum and difference signals at the antenna output ports have some phase relationship, θ. In the case of a real target, the sum and difference signals at the antenna output are almost exactly $\theta + 90^{\circ}$. When tracking a real target, it is desireable to have the sum and difference signals at the receiver mixer output either in phase or 180° out of phase, i.e., colinear. It is for this reason that the channels are calibrated to 90°. The antenna target sum and difference signals at the receiver input have a phase relationship which differs from the real target case by 90°. Therefore, calibrating the antenna target to 90° phase relationship will result in rotating the real target case back to a colinear relationship.

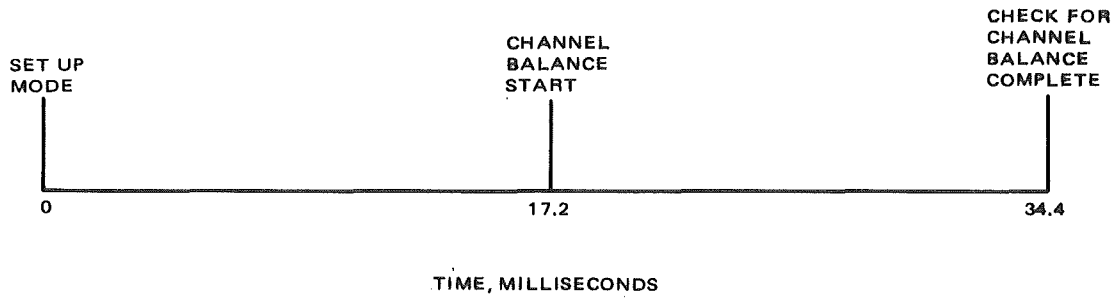

Figure 2.6.3-2. Phase calibration time line.

The figure above indicates the time line for this calibration. At time zero, the antenna target is inserted, and the signal processor (041) is put in HPRF track mode to control the antenna difference channel switches. After 17.2 milliseconds the channel balance start command is sent from the 081 to the 022. After another 17.2 millisecond wait, the BIT software checks for the presence of the channel balance complete signal from the 022. If the signal is present, the calibration is successful. If the signal is not present, a failure is logged. Three successive failures will result in setting the phase calibration fault in the BIT matrix, and in setting NoGo to the BIT Control Panel.

The phase calibration is executed in Initiated BIT, at mode entry to most search and acquisition I modes, and periodically in track, when not inhibited by ECCM considerations.

2.6.4 Amplitude Calibration (Word 8, Bit 2 and Bits 10 – 11)

The objective of the amplitude calibration is to measure the ratio of the difference channel gain to the sum channel gain in the receiver prior to combination as Track 1 and Track 2. Knowledge of receiver gain unbalance is necessary to assure accuracy in track.

The figure below presents a functional block diagram of the combiner circuit in the receiver. Given sum (Σ) and difference (Δ) signals, which are output from the receiver mixers, the combiner circuit forms Track 1 (T1)

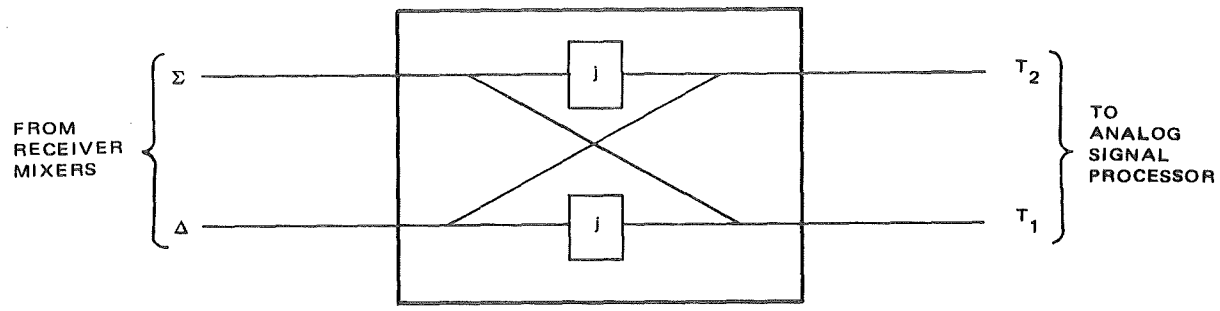

Figure 2.6.4-1. Receiver 90° hybrid combiner.

and Track 2 (T2) when the receiver is in track mode. These are expressed as

$$T1 = \Sigma + j\Delta$$

$$T2 = j\Sigma + \Delta$$

For the amplitude calibration, the receiver is set to track mode, and the antenna target is inserted. The antenna target is inserted into the third quadrant of the antenna, and as a result exits the antenna with sum and difference signals of equal magnitude, i.e.,

$$||\Sigma|| = ||\Delta|| = S$$

As indicated in the section on phase calibration, the phase shifter to the difference channel is adjusted so that when the antenna target passes through the receiver, the two channels have a 90° phase relationship at the mixer output. Therefore,

$$\left.\begin{aligned} \Sigma &= G_{\Sigma}\, S \\ \Delta &= j\, G_{\Delta}\, S \end{aligned}\right\} \text{ at the mixer output}$$

The terms G_{Σ} and G_{Δ} are the pre-combination gains in the receiver sum channel and difference channels, respectively. It is the ratio of these gains

which is to be measured. By substituting the expressions for Σ and Δ into the expressions for T_1 and T_2, they become,

$$T_1 = S\,(G_\Sigma - G_\Delta)$$

$$T_2 = j\,S\,(G_\Sigma + G_\Delta)$$

By taking the vector product of T1 and T2, and dividing by Σ^2 an expression involving only the gains can be written, i.e.,

$$\frac{||T_1 \times T_2||}{\left[\frac{1}{2}(T_1 - j\,T_2)\right]^2} = \frac{G_\Sigma^{\,2} - G_\Delta^{\,2}}{G_\Sigma^{\,2}} = 1 - \frac{G_\Delta^{\,2}}{G_\Sigma^{\,2}}$$

where

$$\Sigma^2 = \left[\frac{1}{2}(T_1 - j\,T_2)\right]^2 = G_\Sigma^{\,2}\,S^2$$

By rearranging the left and right sides

$$\left(\frac{G_\Delta}{G_\Sigma}\right) = \left[1 - \frac{||T_1 \times T_2||}{\left[\frac{1}{2}(T_1 - j\,T_2)\right]^2}\right]^{\frac{1}{2}} = \text{DCAL}$$

which gives an equation for the ratio of sum and difference channel gains as a function of T1 and T2. The square root of the gain ratio, lovingly referred to as DCAL, is stored in the software as the amplitude calibration.

After completion of the amplitude calibration, the value of DCAL is tested. The test limits depend on whether or not the paramp is in the sum channel. The paramp nominally increases the sum channel gain by 5 dB;

therefore, the value of DCAL with the paramp in is nominally 0.562 times the value of DCAL with the paramp out. The limits are:

1. Paramp Out: $0.45 \leq DCAL \leq 2.2$
2. Paramp In: $0.225 \leq DCAL \leq 1.1$
3. FET RCVR: $0.45 \leq DCAL \leq 2.2$

If the DCAL value falls outside these limits, default values of 1.0 paramp out and 0.5 paramp in are used.

In addition, if the test fails in Initiated BIT three times in succession, a failure is marked in the BIT matrix, and a NoGo sent to the BIT Control Panel. In Initiated BIT the amplitude calibration is executed three times with paramp in, and three times with paramp out. If the calibration fails, information is provided in the BIT matrix as to the state of the paramp when the failure occurred. For example, if the calibration failed only with the paramp in, both the amplitude calibration paramp in, and the amplitude calibration failures would be marked in the BIT matrix.

The amplitude calibration is executed periodically in Track Mode, whenever a paramp switch occurs in track mode, and at mode entry in search and Acquisition I modes. When not in Initiated BIT a test failure will only result in substitution of nominal values; no faults are recorded in the BIT matrix.

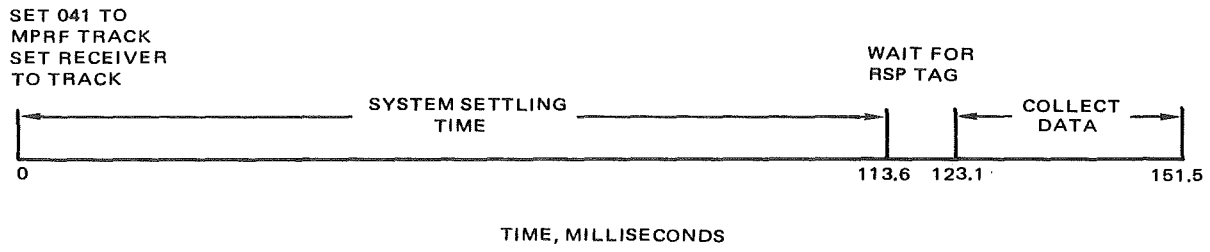

Figure 2.6.4-2. Amplitude calibration time line.

For this calibration, the 041, 022 are placed in MPRF Track Mode, and allowed to settle for 113.6 milliseconds. The settling period is followed by a wait for the RSP tag, which marks the beginning of a data sequence. The

wait for the data sequence may last up to 9.5 milliseconds. The data collection and gain ratio computation then takes another 28.4 milliseconds.

2.6.5 Beacon L.O. Power (Word 8, Bit 6)

The receiver provides the L.O. signal to the IF mixers in beacon mode, and also provides a beacon L.O. power level discrete signal to the Data Processor (081). This signal is meaningful only when the receiver is in beacon mode. This signal is guaranteed set to a logical one state whenever the beacon L.C. power level exceeds 3.7 milliwatt and is within 1 MHz of the desired beacon L.O. frequency, otherwise, it is set to a logical zero state. The nominal power level is 5-20 milliwatts.

The check of this discrete is made every 2 seconds when the receiver is in beacon mode in continuous monitor, and every 100 milliseconds in Initiated BIT. If the discrete is in a logical zero state for three successive checks, the failure is logged in the BIT matrix, and a NoGo is sent to the BIT Control Panel.

2.7 ACQUISITION AND TRACK TESTS (WORD 9, BITS 0 – 1)

2.7.1 Sub-Band 1 and Sub-Band 2 Velocity Search Acquisition Test

This test is designed to check the ability of the system to operate in Velocity Search Mode. In this test the BIT receiver target is inserted into the main channel of the receiver. This data is processed through the receiver (022), the analog signal processor (039) and the digital signal processor (041). The digital signal processor examines this data and provides filter hit data to the data processor (081). The hit data is checked by the BIT software to determine if the hit is in the correct filter.

Figure 2.7.1-1 presents graphically the location and magnitude of the targets. As shown, the search VCO is positioned to 14.88 KHz (below 18.4 MHz). This results in placing one of the receiver targets in filter 58, and one of the receiver targets in filter 314. While there are other targets within the 512 filters, these are the targets of interest for this test.

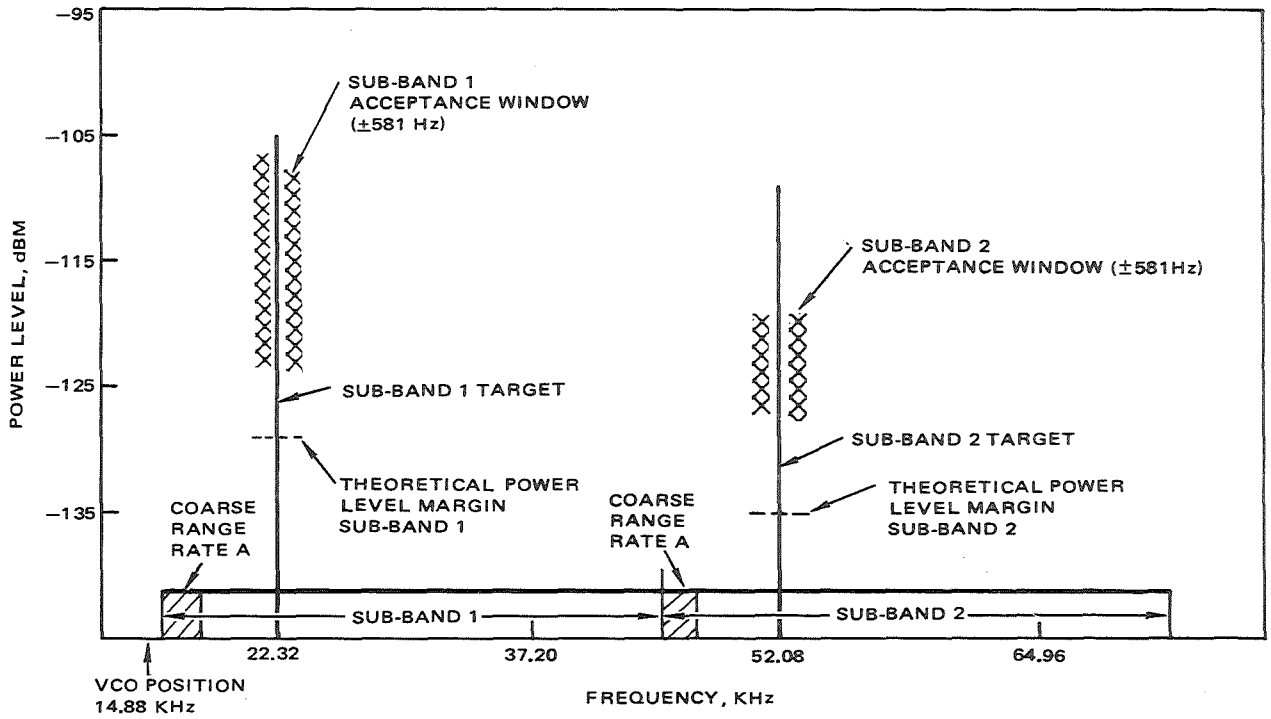

Figure 2.7.1-1. Velocity search acquisition test.

For the sub-band 1 acquisition test, the coarse range rate A is set to filter 20; this will cause the digital signal processor to report to the data processor the first filter hit beyond filter 20. If the sub-band 1 test is to pass, this hit must be in filter 58 ± 5 filters, or equivalently ±581 Hz.

For the sub-band 2 test, the coarse range rate A is increased to 276, so that the digital signal processor will report the first hit above filter 276. In order to pass, the hit must be in filter 314 ± 5.

A failure of the velocity search acquisition test will result whenever either the sub-band 1 or sub-band 2 test fails on three successive times in the same channel. Failure of either the sub-band 1 test or the sub-band 2 test will result in a radar NoGo indication.

Also shown in Figure 2.7.1-1 are the target power levels. Before a hit is recognized in the digital signal processor, it must pass a signal to noise threshold. The thresholds are set by the BIT software so that targets 24 dB (23 dB in sub-band 2) below the nominal will not be recognized. Thus, the acquisition test is a check on system sensitivity.

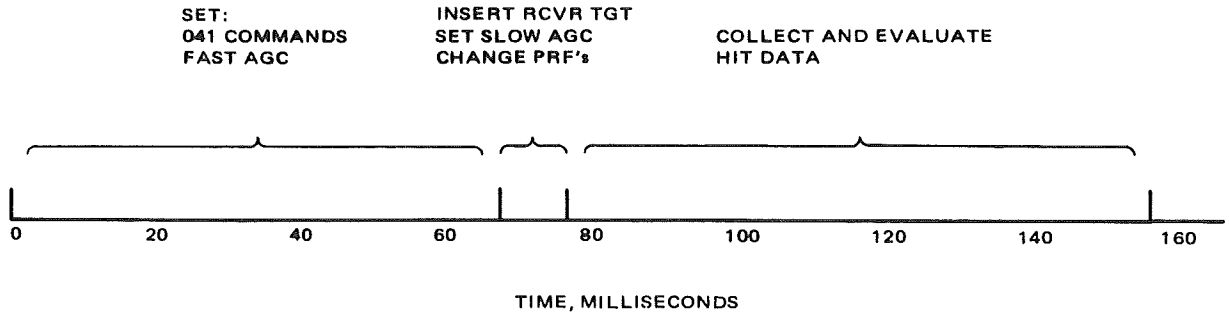

Figure 2.7.1-2. Velocity search acquisition test time line.

The time line above shows the three parts of the acquisition test. The test consumes about 155 milliseconds for this sub-band 1 test and about 155 milliseconds for the sub-band 2 test.

Part one of the acquisition test sets up the system. The digital processor is set to the Acquisition I Mode. In this mode the digital processor will examine the 512 filters for hits, and report them to the data processor.

The VCO is positioned to place the targets in the desired filters; the thresholds are set to provide the desired sensitivity margins; the coarse range rate A is set to exclude undesired targets. The system is set for fast automatic gain control (AGC) and a 67 millisecond wait is started. This wait period accomplishes two purposes:

1. It allows the digital processor to settle after the change of mode to velocity search Acquisition I
2. For analog processors S/N 56 and down, it allows the AGC Loop to settle.

The fast/slow AGC command is not applicable to analog processors S/N 57 and up.

After the 67 millisecond wait, the receiver target is inserted, the AGC is set to slow and the PRF is changed. The PRF is changed for every test so that eventually each of the four HPRFs will have been tested.

Following the insertion of the target, the data collection and evaluation period is begun. While this period lasts for nearly 80 milliseconds, only the data from the final 33 milliseconds is checked for hits. The remainder of the 80 milliseconds is used to allow the target to stabilize. The hit data is examined for correct filter.

At the completion of the sub-band 1 test, the entire 155 millisecond time line is repeated for sub-band 2, with the exception that the coarse range rate A is set to exclude the sub-band 1 targets.

2.7.2 Receiver Blanking Test (Word 9, Bit 4)

The transmitter (011) generates receiver (022) blanking pulses at the PRF during operate, standby and sniff modes. The duration of the blanking pulse is approximately the duration of the transmit pulse. The receiver uses the blanking pulses to actuate blanking gates which attenuate the input signal at both R.F. and I.F. The net result of the attenuation is to close the receiver to all return signals during the transmit pulse.

If for some reason the timing of the receiver attenuation becomes skewed, all or part of the transmit pulse from the GTWT would be seen by the receiver, and consequently, the rest of the system. Such an occurrence

would appear as a high power blast of undesireable noise to the signal processor. The Receiver Blanking Test is used in BIT to detect loss of synchronization between the transmitter and receiver blanking.

The receiver blanking test is the HPRF acquisition test with the GTWT enabled, i.e., the operate command set, and the BIT receiver unblanking command reset. Under these conditions loss of blanking pulse synchronization results in generation of spurious targets, which lie outside the acceptance window, causing a test failure. A failure may also result if the receiver blanking gate permits excessive energy to reach the 039 sub-band AGC circuits thus causing attenuation of BIT targets.

The test is executed only in Initiated BIT. It is executed in channel 6 following the R.F. power tests. The test, like the HPRF Acquisition test looks for a target in sub-band 1, and a target in sub-band 2. The test is executed six times, in the order sub-band 1, sub-band 2, sub-band 1, sub-band 2, sub-band 1, sub-band 2. If the test fails to find the target in the acceptance window in three successive tries out of the six tests, the receiver blanking fault is set in the BIT matrix, and a NoGo is sent to the BIT Control Panel.

2.7.3 Range While Search (RWS) Acquisition Test (Word 9, Bit 2)

The RWS Acquisition test is designed to check the ability of the system to detect and range resolve targets in the RWS mode.

In RWS mode, the R.F. output frequency is ramped so that targets can be distinguished in range by their return frequency.

During phase C, a constant frequency signal is transmitted. Consequently, target returns are different from the transmitted frequency only by the doppler shift of the target. During Phase B, the transmitted frequency is ramped, so that the signal return frequency will differ from the transmitted frequency, not only by the target doppler shift, but by an additional frequency shift resulting from signal delay with range. If the difference between transmit and return frequencies from Phase C is called Δ_C, and the difference between transmit and return frequencies from Phase B is called Δ_B, the difference

$$\Delta = \Delta_B - \Delta_C$$

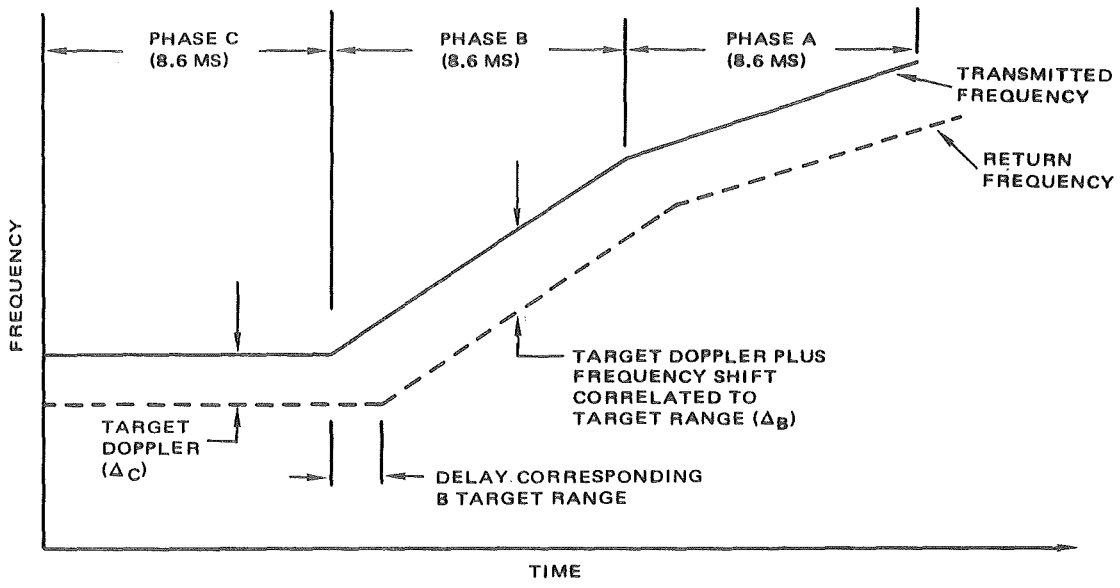

Figure 2.7.3-1. RWS acquisition test ramp.

is the frequency difference corresponding to target range. The digital processor (041) computes this difference, Δ, by determining the frequency shift in the signal return between Phase C and Phase B. This difference is expressed in filters (116.2 Hz per filter) and if confirmed by Phase A, delivers it to the data processor (081), which converts the frequency shift to range (2.09 NMi/filter). During Phase A the slope of the frequency ramp is half of the slope of Phase B. This should result in a frequency shift which is half of the Phase B shift. If it is, the return is confirmed, and data is sent to the 081; if not, it is considered a false alarm, or ghost.

The foregoing describes the method of range determination in the tactical RWS mode. In HPRF mode the BIT receiver target is not delayed in time to simulate range; it is instead pulse modulated to simulate a velocity. This means that the signal input from the BIT receiver target in HPRF mode appears as a number of targets with different velocities at zero range. Therefore, in order to simulate range in RWS BIT test mode, it is necessary to simulate a signal return frequency shift between the phases. This is done by moving the VCO as shown in Figure 2.7.3-2.

During Phase C, the 18.4 MHz VCO is positioned to 16,000 Hz, and the receiver target is inserted into the main channel, which places the receiver targets in filters 47, 175, 303 and 431. During Phase B, the VCO is

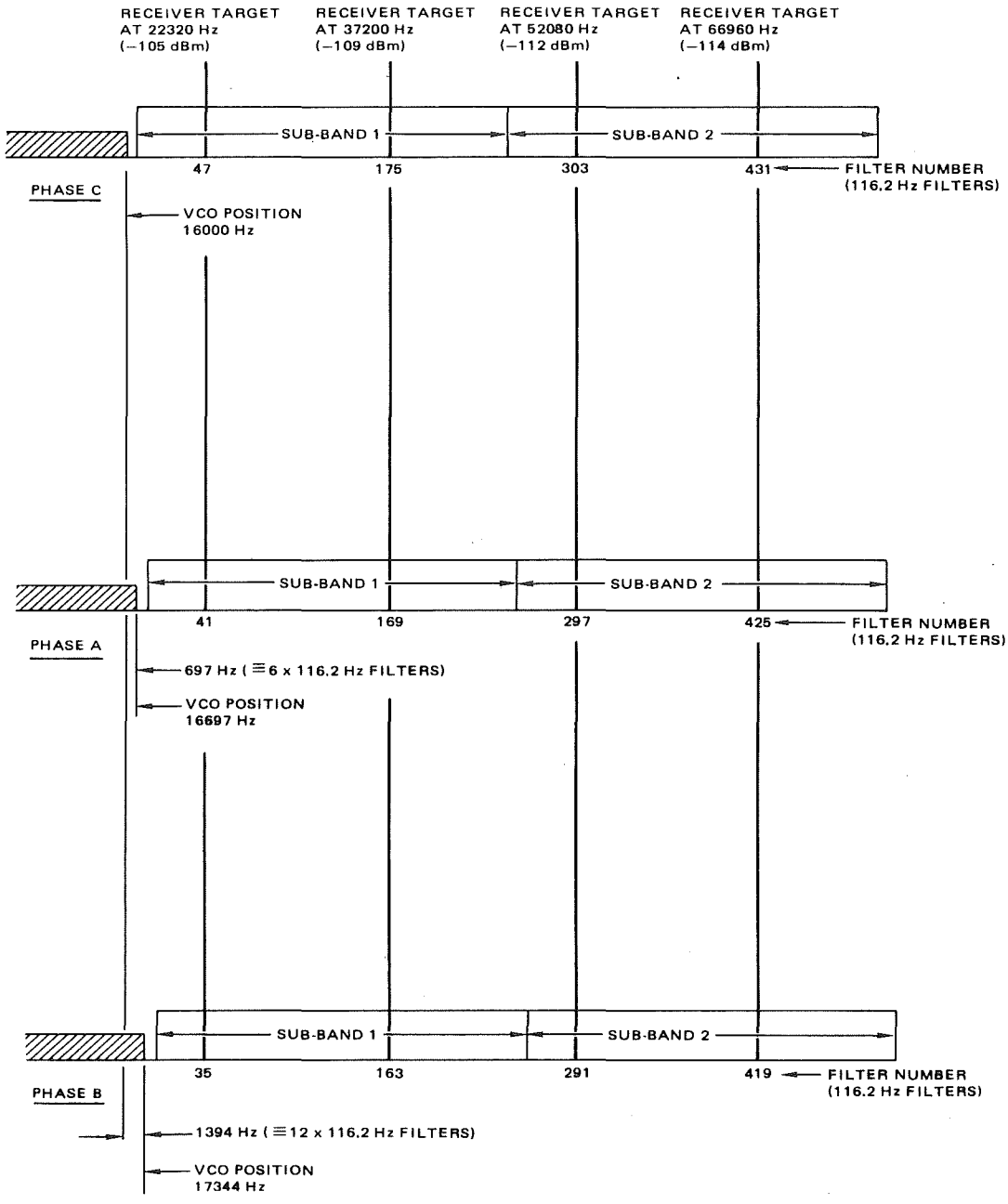

Figure 2.7.3-2. RWS acquisition test.

shifted to 17,394 Hz; this has the effect of moving the targets to filters 35, 163, 291 and 419. The frequency shift for each target is 1,394 Hz, or 12 filters. Phase A confirms these results. The 041 therefore, should detect four targets, with 12 filter frequency shifts, and therefore, should deliver

the number 12 to the 081 as the target range. The target range is measured four times for this test, so that the number 12 should be sent over four measurement periods.

The 081 checks each of these four range measurements against the tolerance 12 ± 5. If any of the four is within this band, the test passes. If all four are outside, the test fails. If the test fails three times in succession, the failure is marked in the BIT matrix, and a NoGo is sent to the BIT Control Panel.

It is interesting to note that because the receiver target appears to be at zero range (unless VCO trickery is used), only the doppler shift of the target is measured during phase A, B, C. This means that if for some reason the FMR ramping would fail, this test would not detect it. Failures of the FMR ramp can only be detected by the FMR ramp test.

The question of test margin is a little complicated in this case, since to fail this test because of weak signal, the system must fail to see all four targets in the two sub-bands. The thresholds have been set in this test so that the receiver target must theoretically be attenuated by 28 dB before the test will fail. As such, this is not much of a test of system sensitivity.

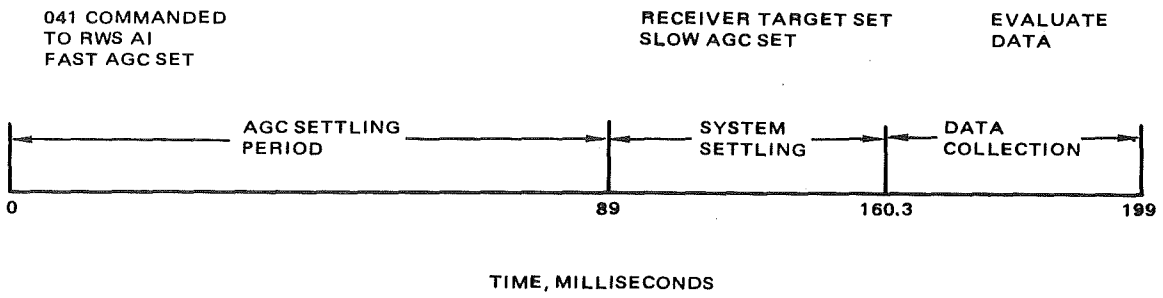

Figure 2.7.3-3. RWS acquisition test time line.

The time line above shows that the RWS acquisition test requires about 199 milliseconds. The first 89 milliseconds are used to allow the 041 to settle into RWS Acquisition I mode, and allows the AGC loop to settle (S/N 56 and down). After this period, the receiver target is inserted, then after another

71.3 millisecond wait to allow the target to stabilize, data is collected for 38.7 milliseconds. At the conclusion of the data collection period, the pass/fail decision is made.

The RWS acquisition test is executed periodically in RWS search mode, and in Initiated BIT.

2.7.4 HPRF Track Test (Word 9, Bit 3)

This test is designed to check the system in HPRF track mode. In this test the BIT receiver target is inserted into the main channel of the receiver. With the receiver (022) and signal processor (039, 041) in track mode, the target information is processed to provide hit/miss data and signal to noise data to the data processor (081).

In this test the 22.8 MHz VCO (which is used only in HPRF track) is positioned to 7.44 KHz (below 22.8 MHz). This will position the -95 dBm receiver target in the center filter (number 18) of the eleven narrow filter bank used in HPRF track. A graph of the location and magnitude of the target is presented below.

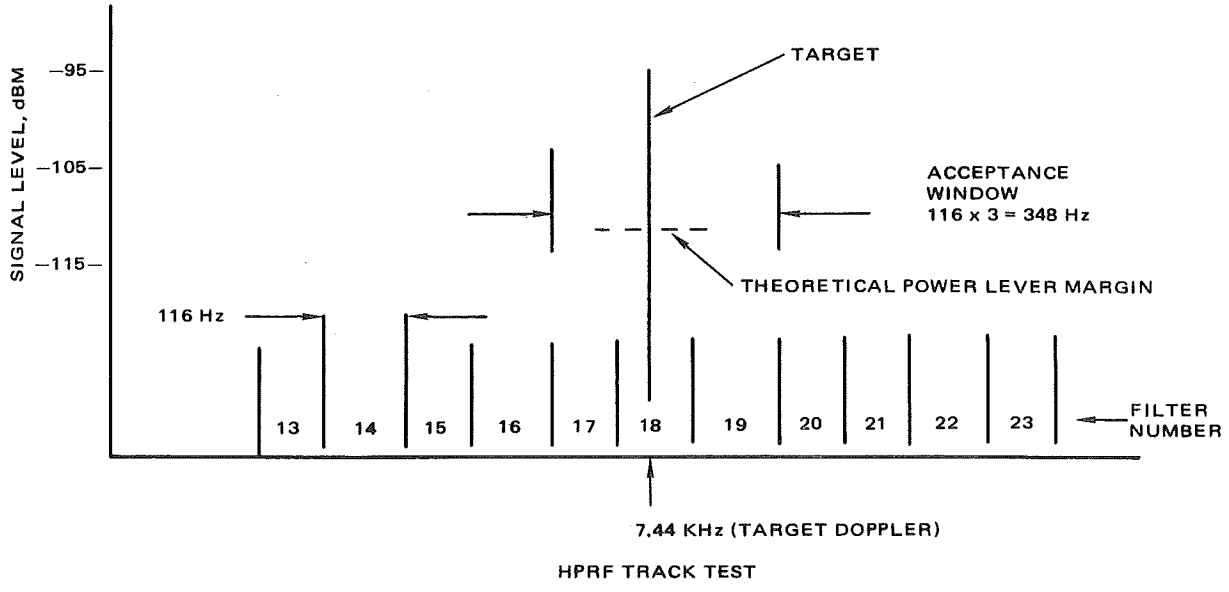

Figure 2.7.4-1. HPRF track test.

To pass this test two conditions must be met in the BIT software, a position test, and signal to noise test. The position test consists of checking the 11 narrow filter hit/miss data. The pass condition for this test is a hit in one or more of three center filters, 17 — 19. The test thus requires that the target be found in a three filter (or 348 Hz) band.

It might be noted that the target must pass a magnitude test before being declared a hit by the digital processor (041). The threshold and gain override levels are set to provide a target which is 16 dB above the signal magnitude required to get a hit. Thus, degraded system gains in processing could result in no hits, and consequently, a failure of the test. In addition, the presence of extra targets within the 11 narrow filters could raise the average signal level within the 11 filters, so that when the digital processor compares the target level to the threshold average signal product, the hit might be lost. In this way the HPRF track test provides a sensitivity check of overall system gain, as well as a check on the presence of spurious targets.

If the hit/miss data indicates that the target is properly positioned in frequency, a signal to noise test is made. This test consists of comparing the signal magnitude in the three center filters (17 — 19) to the signal magnitude in the outlying eight filters (13 — 16 and 20 — 23). If this ratio exceeds 4, the signal to noise is deemed adequate, and test passes. If either the hit/miss target position test or the signal to noise test fails, the entire HPRF track test fails. Three successive failures of this test will result in a radar NoGo indication.

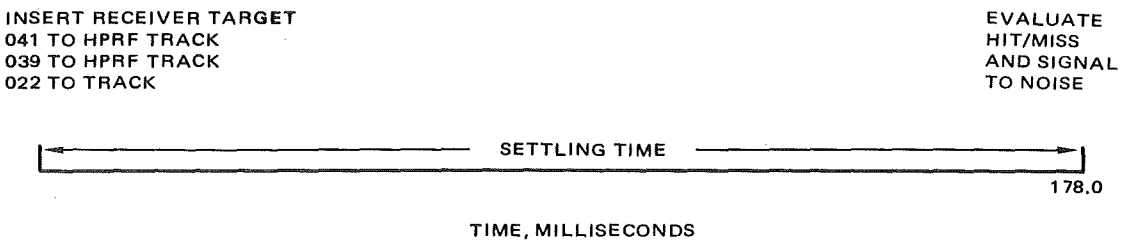

Figure 2.7.4-2. HPRF track test time line.

The time line for this test is presented above. The entire test consumes about 178 milliseconds. The BIT software initiates the test by commanding the digital processor to the HPRF track mode, the receiver to track mode, and by commanding insertion of the receiver target.

At the conclusion of this 178 millisecond period, the hit/miss and signal to noise tests are made.

This test is executed simultaneously with the HPRF gain balance test (see Section 2.7.13) and the 22.8 VCO frequency accuracy test (see Section 2.7.14).

2.7.5 NET2 Test (Word 9, Bit 5)

This test is designed to check the NET2 filter in HPRF mode. The NET2 filter is a 3 KHz wide filter located 62.3 KHz about the 18.4 MHz VCO position. In this test the BIT receiver target is inserted with the system in HPRF Velocity Search Acquisition I Mode. The target data is processed to provide hit or miss indication to the BIT software.

The 18.4 MHz VCO is positioned to 40,500 Hz (about 18.4 MHz). This places the -105 dBm receiver target near the center of the NET2 filter. To pass this test the signal level in the NET2 filter must be 25 dB above receiver noise. If the signal level is adequate, and within the filter, the test passes and the digital processor (041) sends a one bit signal to the data processor (081). Absence of the NET2 indication from the 041 results in a failure.

The NET2 test is the most sensitive of the receiver target tests. The nominal target signal level is 8 dB above the minimum pass level. As such, it is the best check on degraded receiver main channel gain.

The NET2 test is executed only in Initiated BIT when the power switch on the Radar Set Control (541) is in the Operate position. It is executed after completion of the Velocity Search Acquisition I Sub-Band 2 test only in channel 3 when the paramp is in.

The time line for this test is greatly simplified because no mode change is required. The system is already in Velocity Search Acquisition I from the preceding Sub-Band 2 test. This test then consists of positioning

the VCO and waiting 50 milliseconds for the NET2 indication. If no indication is received in 50 milliseconds, the test fails. Three successive failures of the test will result in a radar NoGo indication.

2.7.6 MPRF Acquisition Test (Word 10, Bit 0)

The MPRF acquisition test is designed to test the ability of the system to detect, and range resolve a target in MPRF mode. In this test the digital processor (041) is placed in MPRF Acq I mode, and the receiver is placed in search mode. This has the effect of configuring the signal return system main and guard.

The BIT antenna target is inserted into the antenna, and returns three targets at 6.96 NMi (range bin 86) for the 1.0 microsecond pulse width PRFs, at 9.05 NMi (range bin 112) for the 1.3 microsecond PRFs, and at 11.14 NMi (range bin 138) for the 1.6 microsecond PRFs. Since these three PRFs are alternated in MPRF Acq I, targets at all three ranges should be detected.

At the start of the test, the coarse range A is set to 80. This setting will cause the 041 to discard any targets which are detected below range bin 80. The first target, at 6.96 NMi corresponds to range bin 86. The 041 is commanded to take measurements over four periods, so that if everything goes well, the range bin hit numbers 86, 112, 138 and 86 will be delivered to the 081 over all four measurement periods. The BIT software in the 081 compares each of the four measured hits against the tolerance 86 ± 5. Note that in general only one of the four hits is guaranteed to be from the range bin 86 target, depending on where the sequence starts. For example, it could be 112, 138, 86 or 112. If any of the four targets is in the range bin acceptance band, the test passes, and processing stops.

In none of the four passes, the coarse range A is increased to 107. This will cause the 041 to exclude the first target. The second target is at 9.05 NMi, or range bin 112. Again measurements are recorded over four periods. These might look like 112, 138, 0 or 112. These four measurements are compared to 112 ± 5. If any of the four are within this band, the test passes.

If none of the four passes, the third target is sought by setting coarse A to 130. The 11.14 NMi target should be in range bin 138 ± 5. Again, if any of the four pass, the test passes.

If none of these last four pass, the test fails. If the test fails three times in succession, a failure is marked in the BIT matrix, and a NoGo is sent to the BIT Control Panel.

The thresholds and gain override levels for this test are set to provide a theoretical margin of 21 dB. This means that a loss of gain of 21 dB in the return signal processing should result in a test failure. To this extent, this test is a measure of system sensitivity.

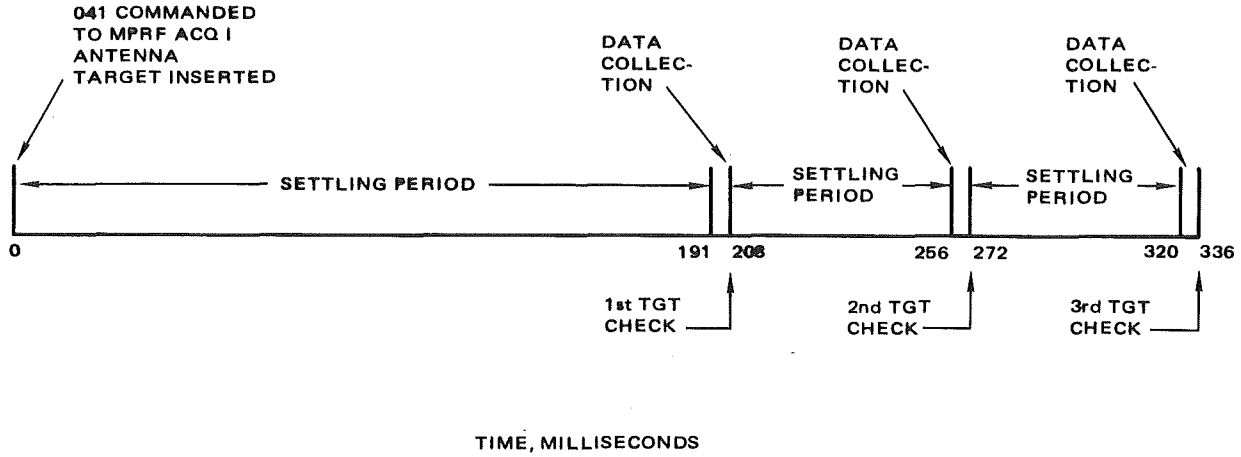

Figure 2.7.6-1. MPRF acquisition test time line.

The time line above is for the MPRF Acquisition test. At the start, the 041 is commanded to MPRF Acq I mode, and the target is inserted. After a 191 millisecond settling period, a 16 millisecond data collection period is begun. At the conclusion of the data collection period, a check is made for the first target. If it is found, the test ends at 208 milliseconds. If not, the test is repeated, looking for the second target. This consists of a 48 millisecond settling period, and another 16 millisecond data collection period. If it fails again, the 48 millisecond, 16 millisecond sequence is repeated for the third target.

The MPRF Acquisition Test is executed periodically at end of bar in MPRF Search Modes, and in Initiated BIT.

2.7.7 LPRF Acquisition Test (Word 10, Bit 1)

The LPRF Acquisition test is designed to detect a target in LPRF mode. In this test, the digital processor (041) is commanded to LPRF Acquisition I mode, and range scale 2X. With the receiver in search mode, this set up will result in the system configured main/guard, and 1.0 microsecond range bins.

The BIT antenna target in this mode will provide a target every 65 microseconds, or 5.24 NMi. At the start of the test, the coarse range A is set to 16, which will cause the 041 to discard any targets below range bin 16. Data is collected over four measurement periods, which should result in collecting four values at range bin 65. The data is compared to 65 ± 5. If any of the four values is in this band, the test passes, and processing stops.

If all four are outside 65 ± 5, the coarse range is increased to 125. Four more measurements are made, the results are compared to 130 ± 5. Again, if any of the four pass, the test passes.

Failing to find the target at range bin 130, the coarse range is set to 190. The hits are checked against 195 ± 5. If none of these last four is in the pass band, the test fails. Three successive failures will result in setting a LPRF acquisition test fault in the BIT matrix, and in setting a NoGo to the BIT Control Panel.

The test margin for the LPRF Acquisition test is 26 dB. This means that a loss of gain of that magnitude should result in a failure. To this extent, this test is a measure of system sensitivity.

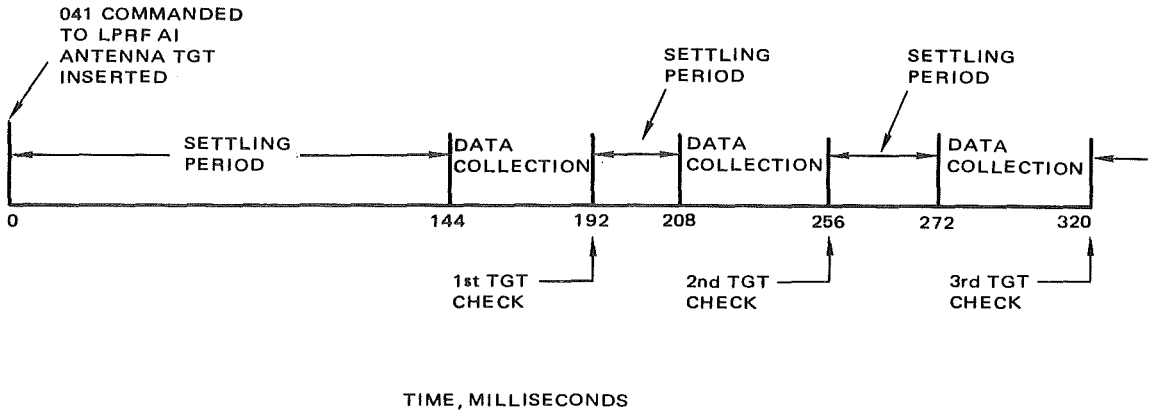

Figure 2.7.7-1. LPRF acquisition test time line.

The 041 is commanded to LPRF Acq I mode and the antenna target is inserted to start the test. After a 144 millisecond settling period, four range bin hit measurements are taken at 12 millisecond intervals. At 192 milliseconds, the hit data is evaluated for the first target at range bin 65. If the hit is satisfactory, the test stops; otherwise it continues after a 16 millisecond settling period to collect four more hits (48 milliseconds), gated to acquire the second target at range bin 130. If this test is successful, the test stops. If still unsuccessful, another 16 millisecond, 48 millisecond sequence is tried.

The LPRF acquisition test executed periodically at end of bar in LPRF search modes, and in Initiated BIT.

2.7.8 Beacon Acquisition Test (Word 10, Bit 2)

The Beacon Acquisition Test is identical in system set up to the LPRF Acquisition Test, except that:

1. The 041 is in short pulse mode
2. The analog processor (039) is in Beacon Mode
3. Only the target at range bin 65 is sought
4. The test is always done in channel 5.

In the tactical Beacon mode, the radar is configured to look for a coded response at a special frequency from an external transponder. Since no provisions have been made for a BIT target with the requisite characteristics to simulate the external transponder, BIT does the best it can in testing the Beacon mode return signal processing by checking the Beacon channel in the 039. Therefore, instead of having the receiver and 041 in Beacon mode as in the tactical case, these units are set up in search and LPRF Acquisition I, respectively.

In this test, the BIT antenna target is inserted into the antenna, with the 041 in LPRF Acquisition I mode, and 039 in Beacon mode. When the 041 is in LPRF mode, the BIT antenna target consists of a string of targets spaced at 65 microsecond intervals, or 5.24 NMi. With the 039 in Beacon mode, the return signal is envelope detected, which should result in targets

every 5.24 NMi, exactly as in the case of the LPRF Acquisition test. For this test, the coarse range is set to always look for the first target at range bin 65, or 5.24 NMi.

As with the LPRF Acquisition Test, data is collected over four measurement periods, which should result in collecting four values at range bin 65. If any of the four is in the band 65 ± 5, the test passes, and processing stops. If none of the four passes, another four values are taken, and the 65 ± 5 test applied again. If none of these passes, a third set of four is taken. If still no acceptable hit has been found, the test fails. Three successive failures result in setting the Beacon Acquisition test failure in the BIT Matrix, and a NoGo to the BIT Control Panel.

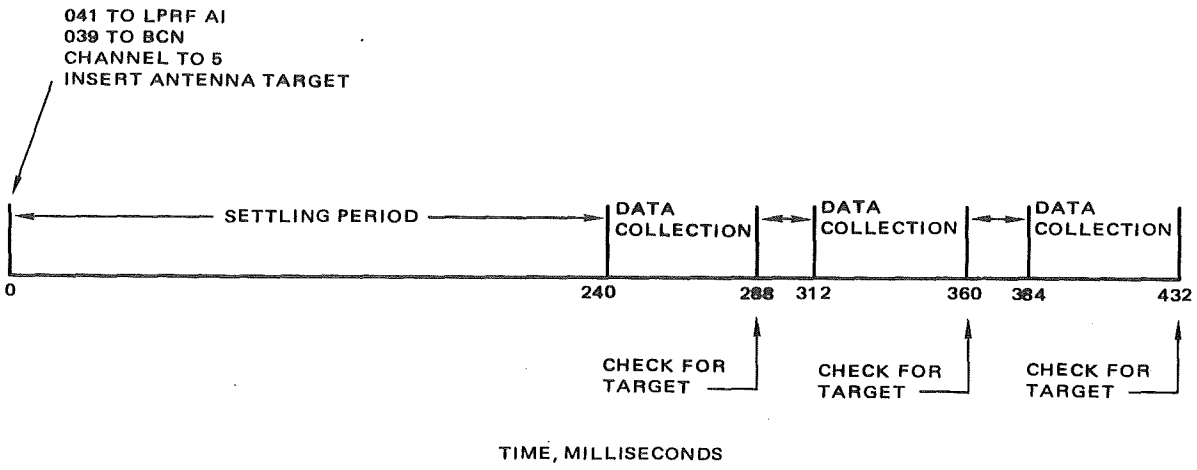

Figure 2.7.8-1. Beacon acquisition test time line.

The time line above shows that the system is allowed to settle for 240 milliseconds prior to data collection. During the data collection period, four data values are taken. If none of these pass, another four are taken over a 48 millisecond period after a 24 millisecond wait. If still none pass, another four are taken, after another 24 millisecond wait. If still no pass value is encountered, the test fails. Therefore, to fail this test one time, no acceptable hit has been encountered over 12 data collection periods.

2.7.9 A/D Converter Gain Balance (Word 8, Bit 9)

This test is designed to evaluate the ability of the 039 A/D converter to convert the two channels of analog signal data to digital form without introducing gain imbalance.

Under normal tactical operation the radar signal data enters the 039 centered about a 30 MHz IF, and is beat down to DC plus signal return doppler. This DC signal is then converted to digital I,Q format by the A/D converter. It is desireable to ensure that conversion to each I or Q be accomplished without changing the relative magnitudes of the input signals.

The A/D converter gain balance test causes the same signal to be inserted into each of the I,Q sampling circuits in analog form. The outputs from each of the A/D converters are then compared in magnitude to determine if they maintained the same relative magnitude.

The input signal to the A/D converters is generated when the BIT software commands Beacon to the 039 unit and MPRF track to the 041 unit. This combination of commands is never used in tactical radar operation, and, in effect, places the 039 in A/D converter test mode.

When the 039 is in this test mode, the normal tactical input lines to the 039 A/D converter sample and hold circuits are disconnected. In addition, an oscillator which operates at 18,801,395 Hz is activated. The BIT software commands the search VCO to output a signal at 18,332,645 Hz. These two signals are beat together, and filtered to produce a signal at 468,750 Hz. This signal is simultaneously input to all four sample and hold circuits of the 039 A/D converter.

For the PRF selected for this test, the A/D converter should output a signal at 5,265.5 Hz with all four I,Q components equal in magnitude.

These four I,Q values are processed through the 041, and transmitted to the BIT software in the 081. The BIT software searches through the four I,Q values and selects the largest of the four, and the smallest of the four, i.e.,

$$\text{Large} = \text{MAX} \begin{pmatrix} I^2 & Q^2 & I^2 & Q^2 \\ T1, & T1, & T2, & T2 \end{pmatrix}$$

$$\text{Small} = \text{MIN} \begin{pmatrix} I^2 & Q^2 & I^2 & Q^2 \\ T1, & T1, & T2, & T2 \end{pmatrix}$$

where

T1 = Track 1

T2 = Track 2

When the largest and smallest values have been selected, the test checks

$$\left| \log_{10} \frac{\text{Large}}{\text{Small}} \right| < 0.5 \text{ dB}$$

i.e., are the largest and smallest values within 1/2 dB of each other?

The test fails if the ratio is in excess of 1/2 dB. If the test fails three times in a row, an A/D converter gain balance fault is set in the BIT matrix, and a NoGo is sent to the BIT Control Panel.

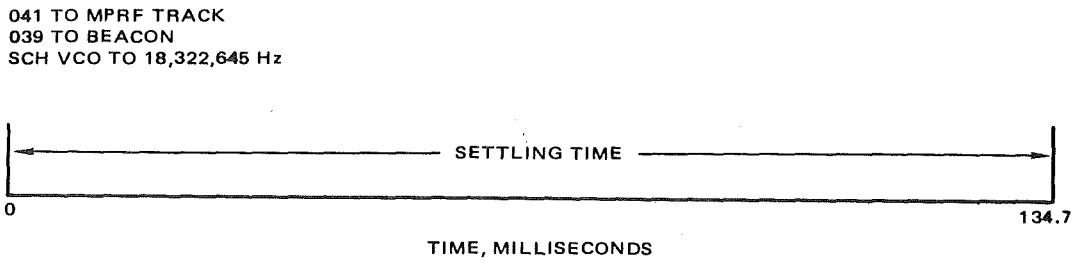

Figure 2.7.9-1. A/D converter gain balance time line.

For this test the 039 is placed in A/D converter test mode when the 041 is commanded MPRF track, and Beacon commanded to the 039. After a settling time of 134.7 milliseconds, the I,Q data is checked for magnitude uniformity.

This test is executed only in Air or Ground Operate Initiated BIT.

2.7.10 MPRF Gain Balance Test (Word 9, Bit 8)

The objective of the MPRF Gain Balance Test is to detect gain imbalances between the two processing channels in the 039, during MPRF mode. A gain imbalance detection of this sort enhances the capability of BIT to distinguish between faults in the 039 unit and the 022 unit.

The desired method to detect gain imbalance would be to insert signals into the Track 1 and Track 2 channels of the 039 which are known to be equal in magnitude. The magnitude of the outputs after conversion to digital would then be compared to determine if the Track 1 and Track 2 signals were still equal in magnitude. Any differences in signal magnitude would then be due to differences in gain in the two channels in the 039.

Unfortunately, the idealized case above is not attainable because the system cannot provide signals which are known to be equal in magnitude at the 039 input. The best that can be done is a known input to the 90^{o} combiner hybrid in the 022 unit.

Thus, this test detects differences in Track 1/Track 2 gain between the input to the receiver track hybrid, and the 039 output. As most of the circuitry between these two points is resident in the 039 unit, failures of this test are attributed to the 039 unit. The preceding discussion has been presented to point out that even though failure of this test is more likely to be a 039 fault, a fault in the 022 or IF cables is not inconceivable.

To accomplish this test, the 041 is commanded to MPRF track mode. The receiver is commanded to track mode, which switches in the 90^{o} hybrid, and the receiver target is inserted into the sum waveguide.

The effect of using the receiver target is to provide a single input to the track hybrid. Since the target is inserted only into the sum waveguide, there is no difference input. Under normal circumstances, the output from the track hybrid is,

$$\text{Track 1} = T1 = \Sigma + j\Delta$$

$$\text{Track 2} = T2 = \Delta + j\Sigma$$

In this case the difference signal, $\Delta = 0$. Thus, the output from the track hybrid is

$$T1 = \Sigma$$

$$T2 = j\Sigma$$

These outputs are then passed through the blanking gates and amplifiers in the 022 unit, and from there input to the 039 through the IF cables.

In the 039 unit, these Track 1 and Track 2 signals are beat down to DC, and output from the 039 as digital I,Q data.

The digital I,Q data is passed through the 041 unit to the 081 unit. Since the data is processed in digital form after exiting the 039 unit, no additional gain imbalance is added after that point.

In the 081, the BIT software computes the sums of squares of the Track 1, I,Q data, and the Track 2 I,Q data over 16 IDA periods. The 16 IDA periods correspond to one full cycle of data at the slow track angle sequence. After the 16 IDA periods, the sums collected are,

$$SUM_{T1} = \sum_{IDA=1}^{16} I^2_{T1} + Q^2_{T1}$$

$$SUM_{T2} = \sum_{IDA=1}^{16} I^2_{T2} + Q^2_{T2}$$

These sums are then compared against the criterion

$$\left| \text{Log}_{10} \frac{SUM_{T1}}{SUM_{T2}} \right| < 5.0 \text{ dB}$$

i.e., do the signal magnitudes in the two channels match to within 2.5 dB?

The test fails if the signal magnitudes are not within 2.5 dB. If the test fails, a failure is noted. Three failures in a row result in a MPRF gain balance fault in the BIT matrix, and a NoGo to the BIT Control Panel.

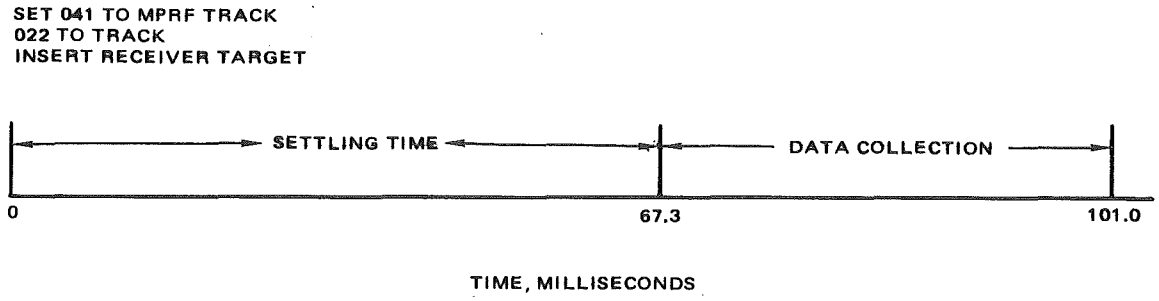

Figure 2.7.10-1. MPRF gain balance time lines.

For this test the 041 is commanded to MPRF track mode using the Major PRF number 7. The receiver is commanded to track modes and the receiver target is inserted. After a 67.3 millisecond settling time (32 IDA periods), a 33.6 millisecond data collection period is consumed. The gain balance computation is made within microseconds of the completion of data collection, so that the entire test uses about 101.0 milliseconds.

This test is executed three times in Air or Ground Operate Initiate BIT, and periodically in A/A search modes.

This test is executed simultaneously with the 18.4 VCO frequency accuracy test (see Section 2.7.11).

2.7.11 18.4 VCO Frequency Accuracy (Word 8, Bit 8)

This test is designed to provide a fine (±100 Hz) check on the positional accuracy of the 18.4 MHz VCO. As with the MPRF gain balance test (Section 2.7.10) the receiver target is inserted and split into Track 1 and Track 2 in the receiver track hybrid. The strategy is to provide Track 1 and Track 2 signals in which the magnitudes are as close as possible to each other at the 039 input. The inserted receiver target is then processed through the 039-041 signal processing chain in the MPRF track mode. The resulting

I,Q data, sent to the 081, is compared by the BIT software for signal magnitude in the two filters of the specified speed gate. A ratio test of the signal magnitude data is applied using the known power roll-off characteristics of the MPRF filters. The pass/fail criterion corresponds to a ±100 Hz mis-positioning of the target in the speed gate.

For this test the 041 is commanded to MPRF track mode. The receiver is commanded to track mode, which switches in the 90^{o} track combiner. The receiver target is inserted into the sum waveguide. The 18.4 MHz VCO is commanded to 18,396,230 Hz, which is 3,770 Hz below 18.4 MHz. The PRF selected for this test is the major of PRF number 7.

The receiver target emerges from the track combiner at 30 MHz as Track 1 and Track 2. Both signals are equal in magnitude and 90^{o} apart in phase, i.e.,

$$\text{Track 1} = \Sigma$$

$$\text{Track 2} = j\Sigma$$

where

Σ = magnitude of receiver target.

These signals are then mixed with 18.4 MHz VCO output at 3,770 Hz below 17.4 MHz to provide a target which should be centered between filters 8 and 9 for the PRF selected.

After an appropriate settling time, I,Q data from this signal processing chain is collected for one IDA period. The BIT software divides the I,Q data into filter 8 data and filter 9 data. The sums of squares of the data from the two filters are then computed,

$$SUM_{f8} = I_{f8}^{2} + Q_{f8}^{2}$$

$$SUM_{f9} = I_{f9}^{2} + Q_{f9}^{2}$$

These sums are then compared to the criterion:

$$\left| \text{Log}_{10} \frac{\text{SUM}_{f8}}{\text{SUM}_{f9}} \right| \leq 3.3 \text{ dB}$$

i.e., do the signal magnitudes match to within 3.3 dB? A study of the power characteristic of the MPRF filters shows that a target which is located more than 100 Hz from the center of the filter 8-9 speed gate will result in greater than a 3.3 dB mismatch in a comparison of signal magnitude.

This test fails if the signal magnitudes are not within 3.3 dB. Three successive failures of this test will result in a 18.4 VCO frequency accuracy fault in the BIT matrix, and a NoGo to the BIT Control Panel.

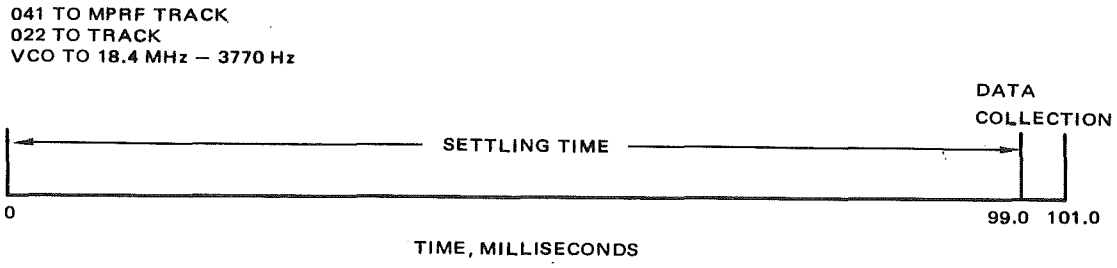

Figure 2.7.11-1. 18.4 VCO frequency accuracy test time line.

After a 99.0 millisecond settling time, data is collected from one IDA period. The signal magnitude comparison test is made within microseconds after the data collection is completed at 101.0 milliseconds. This test is run simultaneously with the MPRF gain balance test.

This test is executed three times in Air or Ground Initiated BIT and periodically in A/A search modes.

2.7.12 MPRF Track Signal Level Test (Word 10, Bit 3)

This test is designed to detect gain imbalances in the receiver ahead of the 90° track combiner. In conjunction with the MPRF gain balance

(Section 2.7.10) and the HPRF gain balance (Section 2.7.13) test, this test is used to distinguish between 039 and 022 faults.

The 041 is commanded to MPRF track mode. The receiver is commanded to search mode, which switches out the 90^{o} track combiner. The antenna target is inserted into one quadrant of the antenna.

The target is split by the antenna waveguide network into a sum signal in the sum waveguide, and a difference signal in the difference waveguide. Since the target is inserted only into one quadrant of the antenna the sum and difference signals are equal in magnitude. Thus, if S is the magnitude of antenna target,

$$\text{SUM} = |\Sigma| = |S + 0 + 0 + 0 + \ |= S$$

$$\text{DIFFERENCE} = |\Sigma| = |(S + 0) - (0 + 0)| = S$$

The difference signal is sent through waveguides directly into the difference receiver mixer. The sum signal may or may not be amplified by the paramp or FET amplifier in the receiver ahead of the sum channel mixer. In Initiated BIT the paramp is out; in continuous monitor the paramp is left in the state dictated by the tactical requirements.

The sum and difference signals emerge from the mixers at IF with a phase difference of approximately 90^{o}. The word approximately is used because the phase difference is not set exactly to 90^{o}m but only to the closest $22\ 1/2^{o}$ step to 90^{o} by the phase balance circuit. Note that the phase difference of 90^{o} is a characteristic of how the antenna target is generated; a real tactical radar target would emerge from the IF mixers with sum and difference signals parallel in phase.

Because the sum and difference signals are both large and have a phase relationship of 90^{o}, they are transmitted to the 039 unit without going through the track combiner, i.e., the receiver is in search mode. Thus, the sum signal is identified as the Track 1 signal, and the difference signal is identified as the Track 2 signal.

These signals are then processed through the 039-041 signal processing chain and sent in I,Q form to the BIT software. The BIT software collects the I,Q data for 16 IDA periods, corresponding to one complete track angle sequence, and computes the magnitude of Track 1 and Track 2,

$$SUM_{T1} = \sum_{IDA\ 21}^{16} I_{T1}^{2} + Q_{T1}^{2}$$

$$SUM_{T2} = \sum_{IDA\ 21}^{16} I_{T2}^{2} + Q_{T2}^{2}$$

These sums are then compared against the criterion

$$\text{Log}_{10} \frac{SUM_{T1}}{SUM_{T2}} \left| \begin{array}{l} \leq 11.0\ \text{dB} \\ \quad 8.5\ \text{dB} \end{array} \right| \begin{array}{l} \text{Paramp in or FET receiver} \\ \text{Otherwise} \end{array}$$

If the gain imbalance is such that this condition is not met, the test fails. Three failures in a row will result in a MPRF track signal level fault in the BIT matrix and NoGo to the BIT Control Panel.

Since the circuits in the 039 are used in computing the magnitude ratio, it might be argued that the source of the gain imbalance cannot be attributed to receiver ahead of the track combiner. If this test were viewed as a stand alone test, such an objection would be well taken. This is not a stand alone test. It is used in conjunction with the MPRF gain balance test (Section 2.7.10) which uses exactly the same 039 circuits. Thus, if the MPRF gain balance test fails, and this test passes, the fault is almost certainly in the receiver.

For this test the 041 is commanded to MPRF track mode using the major PRF number 7. The receiver is commanded to search mode and the antenna target is inserted. After a 67.3 millisecond settling time (32 IDA periods), a 33.6 millisecond data collection period is taken. The gain balance computation is made within microseconds of completion of data collection, so that the entire test uses about 101.0 milliseconds.

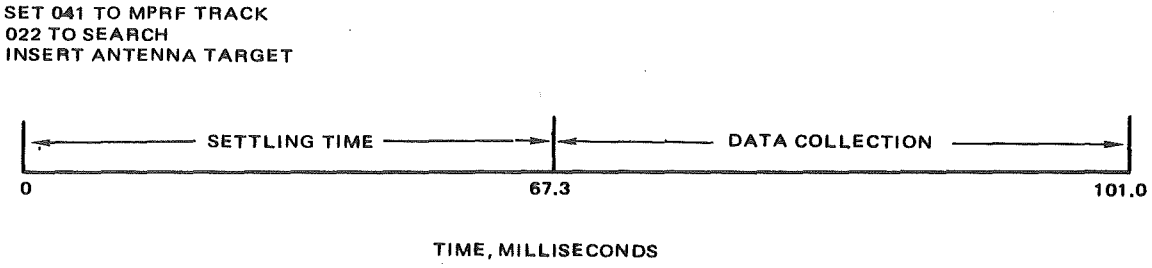

Figure 2.7.12-1. MPRF track signal level time line.

This test is executed three times in Air or Ground Operate Initiated BIT and periodically in A/A search mode.

2.7.13 HPRF Gain Balance (Word 9, Bit 10)

This test is designed to detect gain unbalances in the HPRF Track processing circuits of the 039. Target signals which are as close as possible to each other in magnitude are inserted into the Track 1 and Track 2 inputs to the 039. These signals are processed through the 039-041 signal processing chain and sent to the 081 BIT software as digital I,Q data. The BIT software recombines the I,Q data to determine the signal magnitudes of Track 1 and Track 2. These signal magnitudes are then compared to each other to determine gain unbalance.

To accomplish this test the receiver target is inserted into the sum channel waveguide ahead of the receiver. No signal is inserted into the difference channel. The receiver is commanded to track mode which switches in the 90° track combiner. The track combiner splits the target into Track 1 and Track 2. The output of the track combiner is:

$$\text{Track 1} = T1 = \Sigma$$

$$\text{Track 2} = T2 = j\Sigma$$

i.e., the two signals are equal in magnitude and 90^{o} apart in phase. These signals are then amplified and sent to the 039. If the gains in the receiver amplifiers down stream of the track combiner are equal, these signals should be equal in magnitude at the 039 input.

The ideal method of testing gain imbalance in the 039 would be to insert identical signals at the 039 inputs. Unfortunately, no such test signal is available. Thus, gain imbalance can only be tested from the track combiner input in the receiver through the 039 input. Because most of the circuitry between these points is in the 039, a large gain imbalance is probably a result of a 039 failure.

The 039 is commanded to HPRF track mode. The input signals in this mode are at 30 MHz and carry targets spaced at 14.88 KHz with the first target at 7.44 KHz. The input Track 1 and Track 2 signals are down converted in the 039 to DC to position the 7.44 KHz target in the center of the HPRF track speed gate.

This target is then I,Q detected and converted to digital. The 041 processes this signal in digital form, and transmits it to the 081 BIT software.

The BIT software collects this data for 16 IDA periods, corresponding to one complete track angle sequence. At this time the collected sums are:

$$SUM_{T1} = \sum_{IDA\ 21}^{16} I_{T1}^{2} + Q_{T1}^{2}$$

$$SUM_{T2} = \sum_{IDA\ 21}^{16} I_{T2}^{2} + Q_{T2}^{2}$$

These sums are then compared against the criterion:

$$Log_{10} \left| \frac{SUM_{T1}}{SUM_{T2}} \right| < 5.0\ dB$$

If the Track 1 and Track 2 signals are not within 2.5 dB, the test fails. Three failures in a row result in a HPRF gain balance fault in the BIT matrix, and a NoGo to the BIT Control Panel.

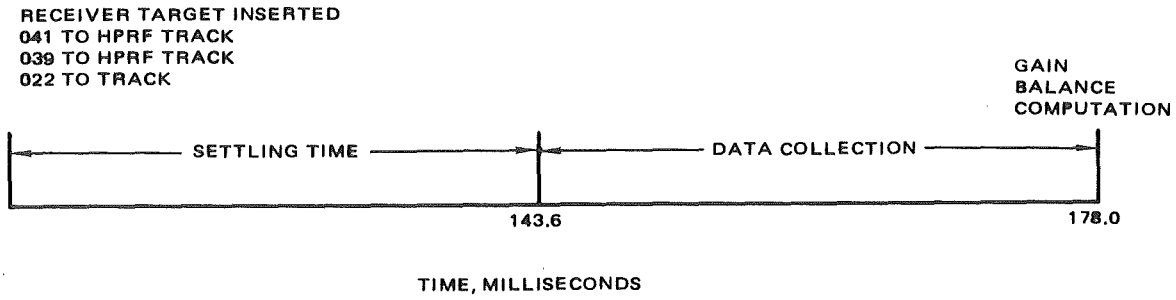

Figure 2.7.13-1. HPRF gain balance test time.

At the start of the test, the BIT software sets up the system mode and inserts the target. After 143.6 milliseconds of settling time, data is collected for 34.4 milliseconds. The gain balance computation is made within microseconds after completion of data collection. Thus, the test requires 178.0 milliseconds. This test is executed simultaneously with the HPRF track test (Section 2.7.4) and the 22.8 VCO frequency accuracy test.

This test is executed three times in Air or Ground Initiated BIT, and periodically in velocity search mode.

2.7.14 22.8 MHz VCO Frequency Accuracy Test (Word 8, Bit 5)

This is the most precise BIT test of the positioning accuracy of the 22.8 MHz VCO. A target at a known doppler frequency is positioned at the center of the HPRF track speed gate. The signal power levels in the two wide filters comprising the speed gate are then compared. The pass/fail criterion for power balance then corresponds to a positioning accuracy of ±100 Hz. Therefore, if the target is within 100 Hz of the center of the speed gate, the test will pass.

For this test the 041 is commanded to HPRF track mode. The 041, in turn, commands the 039 to HPRF track mode. The receiver is commanded to track mode, and the receiver target is inserted into the sum waveguide.

The 041 is also commanded to continuous monitor mode. The combination of continuous monitor command, and HPRF command causes the 041 to send a square wave signal to the transmitter at a frequency of 7.44 KHz. This 7.44 KHz pulse train is mixed with the T.O. signal from the exciter to produce a target spectrum as shown in Figure .

The HPRF track mode command to the 039 activates the 22.8 MHz VCO. The BIT software commands the 22.8 MHz VCO to 7.44 KHz below 22.8 MHz. This should cause the first target at 7.44 KHz to be placed exactly in the center of the HPRF track speed gate, if the VCO goes to position correctly. The HPRF track speed gate corresponds to wide filters (465 Hz/filter) 4 and 5.

The target is processed through the 039-041 chain and is sent to the BIT software as I,Q data. The BIT software computes the target signal level in filters 4 and 5 as follows:

$$S_4 = I_4^2 + Q_4^2$$

$$S_5 = I_5^2 + Q_5^2$$

Signal power levels S_4 and S_5 are computed from data collected over one IDA period. The pass/fail test is:

$$\left| \text{Log}_{10} \frac{S_4}{S_5} \right| \leq 4.5 \text{ dB}$$

The 4.5 dB criterion corresponds to a target 100 Hz away from the center of the filter 4-5 speed gate. This criterion was established using the known power roll off characteristic of the filters.

If this test fails three times in a row, a 22.8 VCO Frequency Accuracy fault is set in the BIT matrix, and NoGo is sent to the BIT Control Panel.

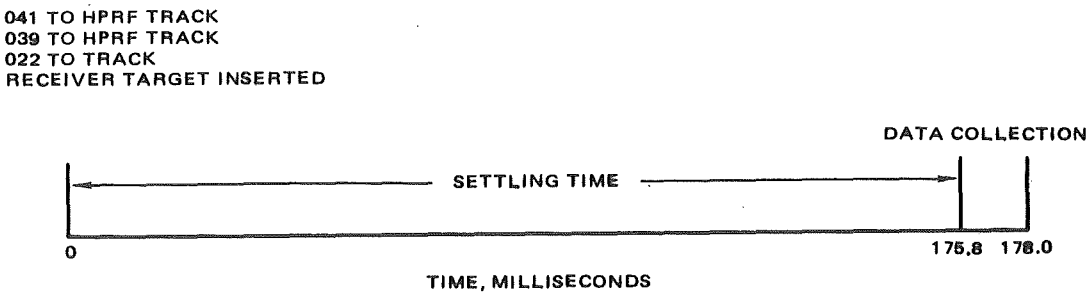

Figure 2.7.14-1. 22.8 MHz VCO frequency accuracy test time line.

After test set-up and a 175.8 millisecond settling time, data is collected over one IDA period. The power level computation is made within microseconds after completion of data collection, so that the entire test takes about 178.0 milliseconds. This test is accomplished simultaneously with the HPRF Gain Balance Test (Section 2.7.13) and the HPRF Track Test (Section 2.7.4).

This test is executed three times in Air or Ground Initiated BIT and periodically in Velocity Search Mode.

2.8 ANTENNA TESTS

The antenna tests are designed to detect faults in the antenna hardware. This includes low voltage power supply (610) servo hardware, as well as the mechanical hardware in the antenna (031). These tests are divided into two parts, Continuous Monitor antenna tests, and Initiated BIT antenna tests.

2.8.1 Continuous Monitor Antenna Tests

The Continuous Monitor antenna tests are passive tests, in that the tests only measure the antenna positions as the antenna moves to satisfy tactical requirements; these tests do not cause antenna motion. The intent of the Continuous Monitor antenna tests is to verify that the antenna is capable of

motion, and is apparently responding to software direction. These tests are not evaluations of antenna control precision, but are intended to detect only a grossly faulty antenna.

The tactical antenna control software is divided into two functions, antenna scanning, and antenna positioning. In antenna positioning tactical requirements dictate placing the antenna at some fixed antenna position. The software computes the azimuth and elevation gimbal drive rates so as to achieve the desired position as quickly as possible, without regard to the path taken to achieve that position. Examples of positioning modes are:

1. Boresight
2. Doppler
3. A/G Ranging
4. Slave Modes
5. Flood
6. Velocity Update
7. Initial Positioning for Scan Modes.

In antenna scanning modes, tactical requirements dictate an elevation bar position, and some range of azimuth over which the antenna is to traverse. The software computes the azimuth and elevation gimbal drive rates so as to maintain the elevation bar position, and to traverse the required azimuth range at some prescribed speed. Examples of scanning modes are:

1. A/A search modes after Initial positioning
2. Acquisition I
3. Supersearch
4. Ground Map
5. Beacon
6. Manual Track.

The Continuous Monitor antenna tests are bypassed under the following conditions:

- Aircraft maneuvers of greater than 6^{o} sec.
- Low Hydraulic Pressure – If the hydraulic pressure in the antenna falls below 275 psi (nominal value 1500 psi) the antenna cannot be expected to scan or position properly. In this case the antenna test bypassed indication (Word 12, Bit 11) is set in the BIT matrix.
- High Roll Rate – If the roll gimbal rate exceeds 25^{o}/second, the Continuous Monitor antenna tests are bypassed, and all antenna test timers are reset.

Assuming none of the three conditions above exist, the Continuous Monitor antenna tests can set one of three faults in the BIT matrix. They are: antenna in position (AIP) fault, roll fault, and scan rate fault.

1. AIP Fault (Word 11, Bit 0) – This fault can occur whenever the antenna control software is attempting to position the antenna. In this test a 7.5 second timer is started whenever the positioning is begun. If the antenna does not achieve a position within 20 milliradians of the desired position simultaneously in azimuth and elevation within the 7.5 second period, the AIP Fault is set in the BIT matrix, and a NoGo is sent to the BIT Control Panel.

   Once the antenna is in position, i.e., within 20 milliradians of the desired position, the 7.5 second timer is stopped. The software then monitors the antenna position every process sync period, and begins the 7.5 second timer again any time the antenna position is outside the 20 milliradian window. If the antenna is continuously outside the desired 20 milliradian window for the 7.5 seconds, an AIP Fault is logged. Three successive 7.5 second failures will result in an AIP Fault in the BIT Matrix, and NoGo will be declared.

2. Roll Fault (Word 11, Bit 4) – This test, executed only during antenna scanning modes, compares the actual roll gimbal position to the desired roll gimbal position. If the roll gimbal is not within 5.625^{o} of the desired position, a fail count is

started. If the count exceeds 243 fails in 400 tries then the Roll Fault is set in the BIT matrix, and a NoGo is sent to the BIT Control Panel.

3. Scan Rate Fault (Word 11, Bit 3) — This fault is set if either the AZ or EL response differs from the command rate by greater than 20 degrees per second 243 times out of 400 tries. If either the AZ or EL channels fail a NO-GO will be sent to the BIT Control Panel, and Scan Rate will be set in Word 11, Bit 3.

2.8.2 Initiated BIT Antenna Tests

The Initiated Bit antenna tests are active tests, in that they cause the antenna to move for test purposes only, and apply pass/fail criteria to the precision of that movement. The tests consist of a low and high rate scan rate test, a roll positioning test, and gyro drift test, and a 610 servo electronics test.

If the antenna hydraulic pressure falls below 275 psi, the antenna sends a low hydraulic pressure discrete to the 081. In such a case the BIT program skips the Initiated BIT antenna tests, and sets antenna test bypassed in the BIT matrix.

2.8.2.1 Low and High Scan Rate Tests (Word 11, Bit 3)

The first test executed is the low rate test. The low rate test is not executed in Air Inititated BIT. In this test the antenna is commanded to use the azimuth and elevation gyros, and the low rate discrete is set. When the low rate discrete is set, the antenna azimuth and elevation drive rate commands are scaled so that a 10 volt command corresponds to 40°/second drive rate. When the low rate discrete is not set, 10 volts corresponds to 150°/second drive rate.

This test begins by commanding the antenna to a position 45° left and 45° down. The antenna is allowed a period of 512 process sync periods (6.40 seconds) to reach a ±20 milliradian window around this position in both azimuth and elevation simultaneously. If the antenna fails to reach this position in the 512 process sync periods, an AIP fault is noted and the test continues. This fault will not be logged as an AIP fault in the BIT matrix unless the next two AIP opportunities in this test fail. In general, an

AIP fault will not be logged in the BIT matrix until three successive AIP opportunities have been missed.

Assuming that the 45° left, 45° down position is reached, the antenna is commanded to a position 45° right and 45° up. The drive command voltage is set to 7.33 volts, which corresponds 29.4°/second in both azimuth and elevation. A 512 process sync period is allowed for the antenna to reach the new position. If the antenna responds properly the antenna should reach the new position in 3.1 seconds.

As the antenna is traversing 45° left, 45° down to 45° right, 45° up, the BIT program monitors the antenna azimuth position. When the antenna azimuth angle crosses 30° left, the software saves the azimuth and elevation antenna positions. These should be near, but to the right of 30° azimuth, and near 30° elevation. At the same time a process sync counter is started. When the counter reaches 178 process sync periods (2.05 seconds), the azimuth and elevation gimbals should have traveled about 60° (at 29.4°/second) from the 30° azimuth position. The elevation and azimuth positions are again recorded, and if the differences between these positions, and the prior stored positions are not 60° ±9° for both azimuth and elevation, a test failure is noted for the low rate test, with antenna moving up and to the right.

From the 45° up, 45° right position, the antenna is commanded to a position 45° down, 45° left. Again a 512 process sync period is allowed to reach this position. While traversing this path, the software again saves the antenna angles when the antenna crosses 30°, this time 30° right. After 178 process syncs, the antenna positions are again recorded, and a 60° ±9° criterion applied to both azimuth and elevation traversals. If the traversed angles are not within the acceptance band, a low rate test with antenna moving down and left is noted. The antenna, meanwhile continues toward the 45° down, 45° left AIP.

At this point an observation is noteworthy:
If the antenna were not capable of movement (as it might not be if the hydraulics were turned off) this would be the third AIP opportunity missed. At this point, an AIP fault would be logged in the BIT matrix, NoGo sent to the BIT control panel, and the scan rate test terminated. This would occur approximately 19.2 seconds into the Initiated BIT antenna tests.

Assuming successful AIP arrivals, the next question considered is did the Up/Right moving low rate test, or the Down/Left moving low rate test fail. If either or both failed, both the Up/Right and Down/Left low rate tests are executed again. The low rate test executed until either both the Up/Right and Down/Left tests pass, or until either test fails three times in succession. If either the Up/Right or Down/Left test fails three times in a row, a scan rate fault is logged in the BIT Matrix, and NoGo sent to the BIT control panel. A scan rate fault and NoGo will terminate the antenna scan rate test. If both tests pass on the first, or any subsequent Up/Right, Down/Left traversal, the antenna scan rate test proceeds to the high rate gyro test.

It should be noted that at the beginning of this test, the antenna is at the 45° down, 45° left position. The high rate gyro test is a duplicate of the low rate gyro test except that the low rate discrete to the antenna servo is reset. This results in the 7.33 volts commanded by this test to result in a 110°/second scan rate. At this faster rate, 65 process syncs (534 ms) is the estimated traversal time for 60°. The same criterion or 60° ±9° is applied. Again, three successive failures of the Up/Right or Down/Left test will result in a scan rate fault, NoGo, and test termination. Passing both the Up/Right and Down/Left tests will initiate the tachometer test. The high rate gyro test is not executed in Airborne Initiated BIT.

In Airborne Initiated BIT the tachometer test is the only scan rate test. This test is identical to the high rate gyro test except that the antenna is commanded to use the azimuth and elevation tachometers, which can only be used at high rate, i.e., 10 volts corresponds to 150°/second. In this case the command voltage of 7.33 volts corresponds to 110°/second, so the time allowed to traverse the 60° is only 65 process sync periods (534 milliseconds). The same criterion of 60° ±9° is applied, and if the test fails scan rate is set in the BIT matrix, and NoGo sent to the BIT control panel.

The above described the average scan rate tests. In addition an instantaneous rate check is made. In the above tests, whenever the antenna is between ±30°, a comparison is made between the antenna rate feedback from the azimuth and elevation gimbals at every process sync period (12.5 ms.). If the difference between the commanded rate and the observed rate exceeds 20°/seconds for either gimbal during any process sync period,

an instantaneous scan rate fault is noted. If, during the antenna scan rate tests, this fault is noted on ten (not necessarily consecutive) process sync periods. A scan rate fault is logged in the BIT matrix and NoGo sent to the BIT control panel.

Concurrent with the azimuth/elevation instantaneous scan rate test, is the instantaneous roll position test. During each process sync of the antenna scan rate tests, a comparison is made of the observed roll position, and the commanded roll position. If this difference exceeds 5.6° for ten (not necessarily consecutive) process sync periods, a roll fault is logged in the BIT matrix, and NoGo sent to the BIT control panel.

2.8.2.2 Gyro Drift Test (Word 11, Bits 1 – 2)

The Gyro Drift test is designed to detect antenna gyros which are unable to hold a stable position under zero drive rate conditions. The gyro drift test is not executed if the antenna ground velocity exceeds 6 NMi/hr.

For this test, the antenna is commanded to switch in the gyros, and the low rate discrete is set. The antenna is allowed to settle in this state for 500 milliseconds. After the settling period, the antenna azimuth and elevation angles are recorded, and a 5 second wait is begun.

At the end of 5 seconds of zero drive rate command, the angles are measured again. If either gimbal has drifted more than 2.5°, the test fails,

and the azimuth and/or elevation gyro drift fault is set in the BIT matrix, and NoGo is sent to the BIT Control Panel.

2.8.2.3 Roll Test (Word 11, Bit 4)

At the beginning of this test, the antenna is brought back to 0^{o} elevation and 0^{o} azimuth. The antenna is allowed 512 process sync periods to reach that position. If it fails to do so, the AIP fault is set in the BIT Matrix, NoGo sent to the BIT Control Panel, and the roll test is skipped.

Assuming the antenna reaches the desired position, a check is made on the weight on wheels discrete, which indicates that the aircraft is on the ground. If the aircraft is not on the ground, the roll test is skipped.

If the aircraft is on the ground, the roll test begins. The roll gimbal is commanded to roll to the left to a position of -95^{o}. A period of 2 seconds is allowed for the roll gimbal to reach a position of -95 ± 5^{o}. If the roll gimbal does not reach this position in the allotted time, the roll test fails, a roll test failure is recorded in the -95^{o} fail counter. [1]

The roll gimbal is commanded to roll to the right, to a position of $+95^{o}$. A period of 4 seconds is allowed for the roll gimbal to reach a position of $+95 \pm 5^{o}$. If the roll gimbal does not reach this position in the allotted time, the fail counter is incremented 1 time for the $+95^{o}$ position. [1]

If the roll gimbal reaches $+95 \pm 5^{o}$, the roll gimbal is commanded to 0^{o}. Again 2 seconds are allowed to reach 0 ± 5^{o}. If not, a failure count for 0^{o} is started. [1] If any position test fails the entire test is started over and a failure declared if 3 fails exist out of three attempts. If a failure is detected (3 fails) a roll rate failure is recorded in the BIT Matrix, and a NoGo is sent to the BIT Control Panel.

[1] T258-1 does not do a 3 times fail check but rather will indicate a fail for a single fail.

2.8.2.4 610 Servo Electronics Test

At this point, the azimuth, elevation, and roll gimbal tests have been completed, and appropriate failures recorded in the BIT Matrix. The 610 servo electronics test is now executed.

For this test the 610 BIT fault isolation test discrete is set by the BIT software. Setting this discrete causes the 610 to output test voltages to the 081 on the antenna feedback analog input lines. The azimuth and elevation tachometers are switched in and the rate feedback voltages are recorded for azimuth, elevation and roll rates. When in test mode, the azimuth command is set to zero volts, the elevation command is set to zero volts and the roll command is set to -0.174 volts. The 610 should produce the following voltages:

Time Seconds	Azimuth (AI04)	Elevation (AI05)	Roll (AI12)
0.25	+6 ± 1.64 Vdc	+3.58 ± 1.22 Vdc	-1.88 ± 1.7 Vdc
0.75	+7.28 ± 2.0 Vdc	+4.34 ± 1.5 Vdc	-2.12 ± 2.0 Vdc
↓	150 Measurements Taken at 10 MS Intervals		↓
2.5	+7.28 ± 2.0 Vdc	+ 4.34 ± 1.5 Vdc	-2.12 ± 2.0 Vdc

Each servo channel is checked at 151 points to evaluate the time response to a step input. The azimuth and elevation channels are checked in a positive going response and the roll channel is checked in a negative going response. This test evaluates the response voltages at a number of points. The table following indicates the pass/fail criteria. If the test voltages fail under those criteria a NoGo is sent to the BIT Control Panel, a 610 Servo Fault is set in the BIT Matrix. The appropriate fault indication is set.

Time of Measurement	Servo Channel in Which Fail Occurred	Set NoGo	Set BIT Matrix					
			Wd 1	Wd 11				
			Bit8	Bit6	Bit7	Bit8	Bit9	Bit10
0.25 Sec	Azimuth	X	X	X			X	
0.25 Sec	Elevation	X	X		X		X	
0.25 Sec	Roll	X	X			X	X	
0.75 Sec	Azimuth (≥10 fails in 150)	X	X	X				X
thru	Elevation (≥10 fails in 150)	X	X		X			X
2.5 Sec	Roll (≥10 fails in 150)	X	X			X		X

All tests which fail will be indicated in the BIT Matrix and no tests are bypassed upon failure of a previous test.

Upon completion of the above tests, the 081 sets the 610 back to its zero or no input condition. A command to each servo input which is exactly equal and opposite to the step response created by the test mode switching is sent. These inputs to produce a zero balance output are as follows.

- Azimuth +1.42 Vdc
- Elevation +1.42 Vdc
- Roll -0.140 Vdc

After a 1 second delay, the 610 should produce the following voltages:

- Azimuth 0 ± 0.6 Vdc
- Elevation 0 ± 0.6 Vdc
- Roll 0 ± 1.2 Vdc

If the test voltages are outside these limits, the following BIT Matrix and NoGo setting will occur.

Fail Channel	NoGo Set	Wd 1 Bit8	Wd 11 Bit6	Wd 11 Bit7	Wd 11 Bit8	Wd 11 Bit11
Azimuth	X	X	X			X
Elevation	X	X		X		X
Roll	X	X			X	X

With the servo at zero balance (assuming no failures) the 610 is commanded into another step response condition to evaluate the ability of each servo to respond to the opposite going step condition, i.e., azimuth to negative step, elevation to negative step and roll to a positive step. These steps are produced by inputting a step voltage to the command inputs of each servo which is equal and opposite to the original step response produced by the 610 test mode command. These step inputs are Az = 2.84v, El = 2.84v and Roll = -.110v. The 610 should produce the following voltages:

Time Seconds	Azimuth (AI04)	Elevation (AI05)	Roll (AI12)
0.25	-6 ± 1.64 Vdc	-3.58 ± 1.22 Vdc	+1.88 ± 1.7 Vdc
0.75	-7.28 ± 2.0 Vdc	-4.34 ± 1.5 Vdc	+2.12 ± 2.0 Vdc
↓	150 Measurements Taken at 10 MS Intervals		↓
2.5	-7.28 ± 2.0 Vdc	-4.34 ± 1.5 Vdc	+2.12 ± 2.0 Vdc

As indicated, each servo channel is checked at 151 points to evaluate the time response to a step input. In this case, the step response is exactly equal and the opposite to that in the first sequence of tests, thus insuring the smooth operation of antenna drive in both directions. If the test voltages are outside these limits for the number of times indicated, the following matrix and NoGo settings will result.

Time of Measurement	Servo Channel in Which Fail Occurred	Set NoGo	Set BIT Matrix					
			Wd 1	Wd 11				
			Bit8	Bit6	Bit7	Bit8	Bit9	Bit10
0.25 Sec	Azimuth	X	X	X			X	
0.25 Sec	Elevation	X	X		X		X	
0.25 Sec	Roll	X	X			X	X	
0.75 Sec	Azimuth (≥10 fails in 150)	X	X	X				X
thru	Elevation (≥10 fails in 150)	X	X		X			X
2.5 Sec	Roll (≥10 fails in 150)	X	X			X		X

The above sequence concludes all of the tests using tachometer mode. The next sequence tests the gyro mechanization for azimuth and elevation by using a similar step response technique. The 610 is set back to its normal non-test configuration and gyros are commanded to the servo channels (roll channel is gyro only). The 610 is allowed to reach steady state conditions with zero command rates to the azimuth and elevation channels and -0.174 Vdc to the roll command. This stable state is assumed to have been reached after a delay of 1 second. Upon reaching this stable state, the 610 is again commanded to the test mode and the 610 voltage responses measured as shown below.

Time Seconds	Azimuth (AI04)	Elevation (AI05)
0.25	+1.85 ± 1.2 Vdc	+2.79 ± 1.2 Vdc
0.75	+2.46 ± 1.5 Vdc	+3.85 ± 1.5 Vdc
↓	150 Measurements Taken at 10 MS Intervals	↓
2.5	+2.46 ± 1.5 Vdc	+3.85 ± 1.5 Vdc

As indicated above, each servo channel is checked at 151 points to evaluate the time response to a step input. If the test voltages fall outside the limits for the number of times indicated below, NoGo and the following matrix indications will result.

Time of Measurement	Servo Channel in Which Fail Occurred	Set NoGo	Set BIT Matrix					
			Wd 1	Wd 11				
			Bit8	Bit6	Bit7	Bit8	Bit9	Bit10
0.25 Sec	Azimuth	X	X	X			X	
0.25 Sec	Elevation	X	X		X		X	
0.25 Sec	Roll	X	X			X	X	
0.75 Sec	Azimuth (≥10 fails in 150)	X	X	X				X
thru	Elevation (≥10 fails in 150)	X	X		X			X
2.5 Sec	Roll (≥10 fails in 150)	X	X			X		X

This sequence concludes the testing of the antenna servo except for the buffered PSD output checks to follow. No measurement is possible for response to a negative step in gyro mode due to the inability to input a command torque when gyro is selected in either azimuth or elevation. This limitation is caused by internal switches but does not present a problem since all circuit functions are common between gyro and tachometer mode except for the compensation capacitors and resistors which do not exhibit a directional bias.

While still in the test mode and with gyros selected, the buffered azimuth PSD and buffered elevation PSD outputs are measured and compared against the following limits:

Buffered Az PSD = +1.54 ± 0.2 Vdc

Buffered El PSD = +1.54 ± 0.2 Vdc

If either or both PSD voltages fall outside the limits, the following NoGo and Matrix conditions will be set.

	NoGo	Wd 1, Bit8	Wd 11, Bit6	Wd 11, Bit7
Az PSD	X	X	X	
El PSD	X	X		X

This concludes the 610 servo self test sequence and will isolate any failures during the test to the 610 Servo Electronics. If the 610 servo self test passes and there were any failures in:

- Antenna in position
- Azimuth Gyro drift
- Elevation Gyro drift
- Scan rate, or
- Roll rate

the fault will be isolated to the 031.

2.8.3 Az/El Diode Switch Fault (Word 11, Bit 5)

The antenna Az/El diode switch is used when the antenna is in track mode. The position of the switch determines whether the difference signal output from the antenna is left and right (azimuth) difference, or upper and lower (elevation) difference. The position command is supplied by the radar signal processor (041) unit. The drive power for the switch is derived from a -21 volt supply emanating from the 610 unit.

The most frequency failure mode of the Az/El diode switch is a short circuit. When the switch shorts, the -21 volt supply is typically pulled up to a -17 volts.

In order to detect this fault, a circuit has been installed in the 610 unit which monitors the -21 volt supply. If the voltage increases above -18 volts the 610 unit sets the 610 fault indicator. The setting of the fault indicator simultaneously sets the 610 fault indicator discrete input line to the 081 unit.

The BIT software monitors the 610 fault indicator discrete input line every process sync period in all BIT modes and all tactical modes. If the fault indicator is set, the BIT software checks the 610 operational discrete input. The 610 operational discrete is a signal sent by the 610 to the 081; a set state implies that the 610 is alive and well, a reset state means a faulty 610. A 610 failure will result in resetting the 610 operational discrete, and in setting the 610 fault indicator discrete. Thus, a set fault indicator could mean either a not operational 610 or a shorted Az/El diode switch in the antenna. The check of the 610 operational discrete resolves this ambiguity. If the 610 is operational, the setting of the fault indicator must be due to Az/El diode switch failure.

If the Az/El diode switch fails, the Az/El diode fault is set in the BIT matrix, the antenna (031) fault is set in the BIT matrix, and NoGo is sent to the BIT Control Panel.

The Az/El diode test is executed every process sync period. One failure of the test results in a NoGo.

2.9 BIT MATRIX INDICATORS

2.9.1 Air Initiated BIT and Ground Initiated BIT Indicators (Word 12, Bits 9 – 10)

Two indicators, "GBIT RUN" and "ABIT RUN", have been provided in the BIT matrix. The primary purpose of these indicators is to inform matrix watchers:

1. Whether this Initiated BIT data is a result of Air Initiated BIT testing or Ground Initiated BIT testing
2. Whether or not the Initiated BIT data is a result of an Initiated BIT test executed before or after the radar last went through power up.

The indicators are set or cleared in the two BIT matrices according to the following rules:

1. Both indicators in Continuous Monitor BIT Matrix are cleared (set to zero) at power up, and only at power up
2. Both indicators in the Initiated BIT Matrix are cleared at the beginning of Initiated BIT and only at the beginning of Initiated BIT
3. The "ABIT RUN" indicator is set in both the Continuous Monitor BIT Matrix and the Initiated BIT Matrix at the conclusion of an Air Initiated BIT test sequence
4. The "GBIT RUN" indicator is set in both the Continuous Monitor BIT Matrix and the Initiated BIT Matrix at the conclusion of Ground Initiated BIT test sequence.

These rules are translated into the exhaustive set of output combinations listed in Table 2. 9. 1-1.

TABLE 2.9.1-1. OUTPUT COMBINATIONS OF "ABIT RUN" AND "GBIT RUN" INDICATORS

Matrix	GBIT Run	ABIT Run	
IB	—	—	Last Initiated BIT not completed (No I-BIT read out).
CM	0	0	No Initiated BIT executed since power-up.
IB	—	—	Last Initiated BIT not completed (No I-BIT read out).
CM	1	0	Only Ground Initiated BIT was run since power-up.
IB	—	—	Last Initiated BIT not completed (No I-BIT read out).
CM	0	1	Only Air Initiated BIT was run since power-up.
IB	—	—	Last Initiated BIT not completed (No I-BIT read out).
CM	1	1	Both Air and Ground Initiated BIT run since power-up.
IB	0	1	Last Initiated BIT run was Air Initiated BIT.
CM	0	1	Only Air Initiated BIT was run since power-up.
IB	1	0	Last Initiated BIT run was Ground Initiated BIT.
CM	1	1	Both Air and Ground Initiated BIT were run since power-up.
IB	0	1	Last Initiated BIT run was Air Initiated BIT.
CM	1	1	Both Air and Ground Initiated BIT were run since power-up.
IB	1	0	Last Initiated BIT run was Ground Initiated BIT.
CM	0	0	Initiated BIT results were taken prior to last power-up.
IB	0	1	Last Initiated BIT run was Air Initiated BIT.
CM	0	0	Initiated BIT results were taken prior to last power-up.

NOTE: 1. IB = Initiated BIT Matrix
CM = Continuous Monitor BIT Matrix

2. No other combinations are possible.

3.0 BIT TRACK TEST

The term track test is a misnomer, since track is only part of it, and it is not a test. Track test is a qualitative capability check of the radar; its intent is to provide the radar operator with a means of exercising both hardware and software radar components without resorting to use of external target generators. For track test the BIT receiver target is used in place of an external target generator. The normal radar controls can then be used to acquire and track this target.

Track test is not really a test in the sense that it can be passed or failed. Track test cannot set the radar NoGo light, it is a qualitative test which provides the operator with confidence that the radar set can detect, acquire and track a target.

3.1 INITIATION AND TERMINATION OF TRACK TEST

Track test can be entered only from air or ground operate initiated BIT. Eight seconds after the operator has entered air or ground Initiated BIT, the words "TK TST" will appear in the VSD BIT window. "TK TST" will be displayed for eight seconds if no action is taken by the operator. If at any time during the eight second "TK TST" display the operator selects Supersearch or Vertical Scan from the flight control stick, the radar set will enter track test mode. While in track test mode, "TK TST" will remain in the VSD BIT window. Once the track test mode, the radar should appear to be in a tactical radar operating mode. For example, in the air to air search modes, the antenna should swing; the system should respond to changes in antenna scan pattern commands and range scale command from the 541; targets should appear on the VSD in all air to air search modes and in Ground Map.

Track test will be terminated when the operator next enters Initiated BIT, whether in standby, operate, air or ground modes. Track test is also automatically terminated in the event of a missile launch.

When in track test, BIT notifies the CC by setting the track test bit (CC Message 3, Word 2, Bit 8).

3.2 TRACK TEST TARGET GENERATION

For track test BIT alters the normal tactical operating set up of the radar as follows:

1. SNIFF command to the transmitter is set. This precludes the possibility of generating any RF output from the GTWT during track test.
2. Interceptor Velocity (V_I) is set to 812 FPS. This establishes a side lobe clutter value which is used to position the track test targets in Velocity Search (VS) mode.
3. BIT Receiver Unblanking is set. This allows the track test target to enter the receiver.
4. The 041 unit is commanded to continuous monitor (CM) commanding the 041 unit to CM mode. This alters the signal (sent from the 041 to the 011) on the PRF trigger line as a function of PRF. This signal controls gating of the GTWT drive from the exciter. By appropriately gating the GTWT drive, the BIT target is generated. The generation of the BIT target varies as a function of mode as follows:
   a. LPRF – The GTWT drive is gated on every 65 microseconds. This results in a target every 5.24 NMi.
   b. MPRF – The GTWT drive is gated on at range bin 22 for the 64 bin PRFs, range bin 20 for the 66 bin PRFs, and range bin 18 for the 68 bin PRFs. This scheme results in a target which resolves at range bin 86. For the three search PRFs, the targets appear at 6.96 NMi, 9.05 NMi and 11.14 NMi.
   c. HPRF – The GTWT drive is modulated by a 7.44 KHz square wave. This modulation generates a target spectrum which forms discrete targets at 14.88 KHz intervals. (See Figure 5.3.1-1.)

   Samples of typical target patterns on the VSD are presented in Figures 3.2-1 and 3.2-2.

It should be noted that generation of the BIT target is not of itself sufficient to enter the target in the signal processing stream. The final step required is command of target insertion.

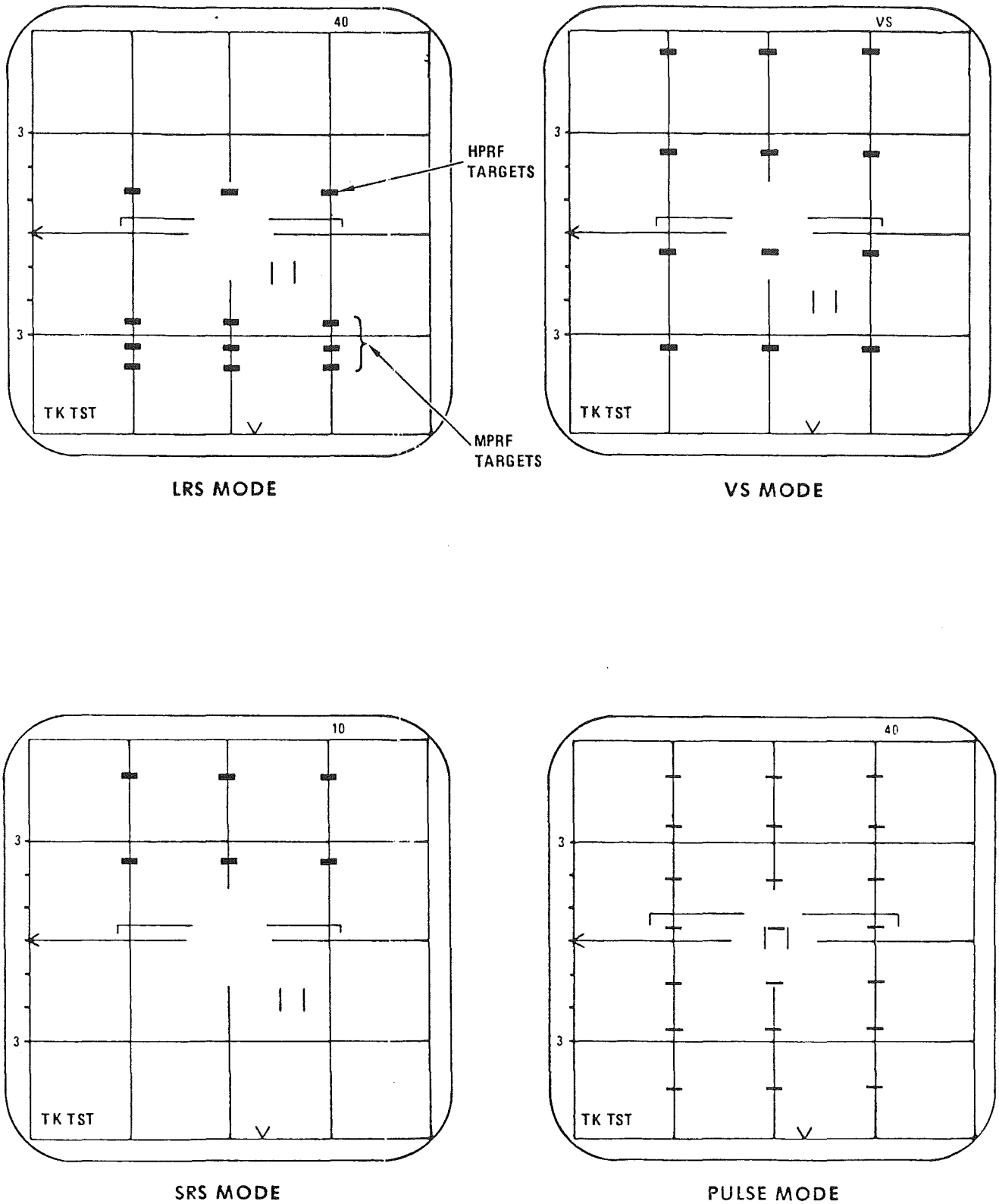

Figure 3.2-1. Search displays.

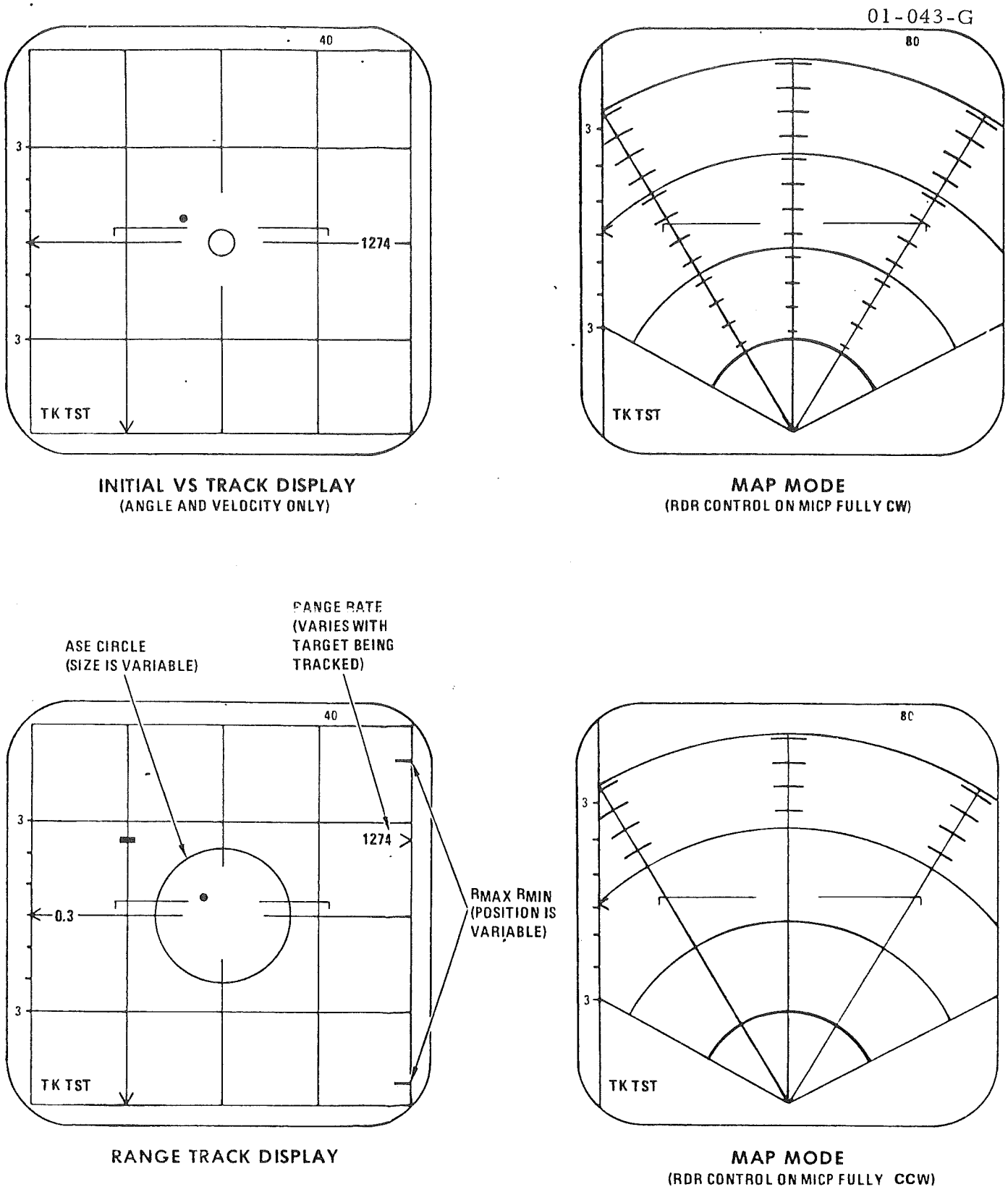

Figure 3.2-2. Typical track displays and MAP displays.

Having altered the normal tactical set-up of the radar as described in the four items above, target insertion is the final set-up required before the target can be processed and displayed on the VSD. The target is inserted into the main channel waveguide upstream of the receiver whenever the BIT software sets the BIT receiver target command. The BIT receiver target command is set as a function of antenna position according to the following rules.

The target is inserted whenever conditions 1 and 2 below are satisfied:

1. Absolute value of elevation angle less than 3.86^{o}
2. Absolute value of azimuth angle less than 1.76^{o} or absolute value of azimuth angle between 29.52^{o} and 33.39^{o}.

Satisfying both of these criteria will thus display targets near the 0^{o} elevation bar at azimuth angles near 0^{o}, $+30^{o}$ and -30^{o}.

3.3 TRACK TEST USAGE

Once in track test mode, and having set the antenna scan controls according to the rules described above, the operator should see targets displayed on the VSD. Typical examples are shown in Figure 3.2-1 and 3.2-2.

In HPRF and MPRF modes, these targets may be acquired and tracked to get the track displays as shown in Figure 3.2-2. The MPRF modes include Supersearch, Gun Scan and Boresight.

When tracking the BIT target, several deviations from tactical tracking modes are made.

Burst rangings are deleted. The purpose of burst rangings in tactical HPRF track is to determine the range to the target. The BIT receiver target is at zero range, so no information could be provided by a burst ranging. Instead, track test sets a constant range of 24 NMi for HPRF track.

In MPRF track burst rangings are made to locate the altitude line and to eliminate jet engine modulation (JEM) lines. Since the system is tracking the BIT target, JEM lines are not a problem.

The location of the altitude line is important in tactical MPRF track for PRF selection. The BIT target is clear in all PRFs, so no PRF switching is done. The PRF sorting and ranking logic is disabled.

In tactical tracking mode, the system performs angle tracking by measuring azimuth and elevation difference signals from the antenna. The discriminants computed from these difference signals are used to compute antenna position corrections to maintain track. In the case of the BIT target no difference signal from the antenna exists, i.e., the difference signal is zero regardless of where the antenna points.

In order to maintain a solid antenna position in track test track, a track test angle discriminant is formed. This discriminant creates error parameters which are proportional to the difference between the current antenna position and the antenna position at which the target was acquired. This discriminant is scaled to be comparable in magnitude to the tactical angle discriminant, and fed into the tactical angle tracking algorithm.

With the exception of these modifications, the track test exercises the complete tactical search, acquisition and track software. In addition, with the exception of major parts of the 011 unit which deal with generation of RF power, the track test exercises most of the radar hardware.

4.0 BIT TIMING

4.1 INITIATED BIT TIMING

This section presents timing data for Initiated BIT modes. Standby Initiated BIT modes are used to read out BIT matrix data. The timing for Standby Initiated BIT modes simply consists of displaying non-zero BIT matrix words for 7.5 seconds each.

The timing for the Operate Initiate BIT modes is presented in Figure 4.1-1. The figure presents the sequence of tests executed in Initiated BIT and a time required for each test. The times for the various tests are presented in the column at the right. The figure also presents a more detailed breakdown of how the execution time of each test is used.

The sequence of tests in Figure 4.1-1 is presented in the order in which the tests are executed in Initiated BIT. Only the relatively large time consuming activities are shown. There are some activities, which are important, but which require very little time. Examples of these activities are clearing of BIT matrix and Fault Isolation. These activities require times on the order of hundreds of microseconds; for this reason, they are not listed in the Initiated BIT time line. Table 2.1 presents a listing of the major Initiated BIT activities in the order of execution.

Ground/Operate Initiated BIT executes all tests. Some of these tests are not executed in Air/Operate Initiated BIT. These exceptions are noted in Figure 4.1-1 and in Table 2.1.

The times presented are nominal values, which assume a radar system which passes all tests. Test failures can, in some cases, significantly extend the execution times. The time lines presented are not drawn to scale.

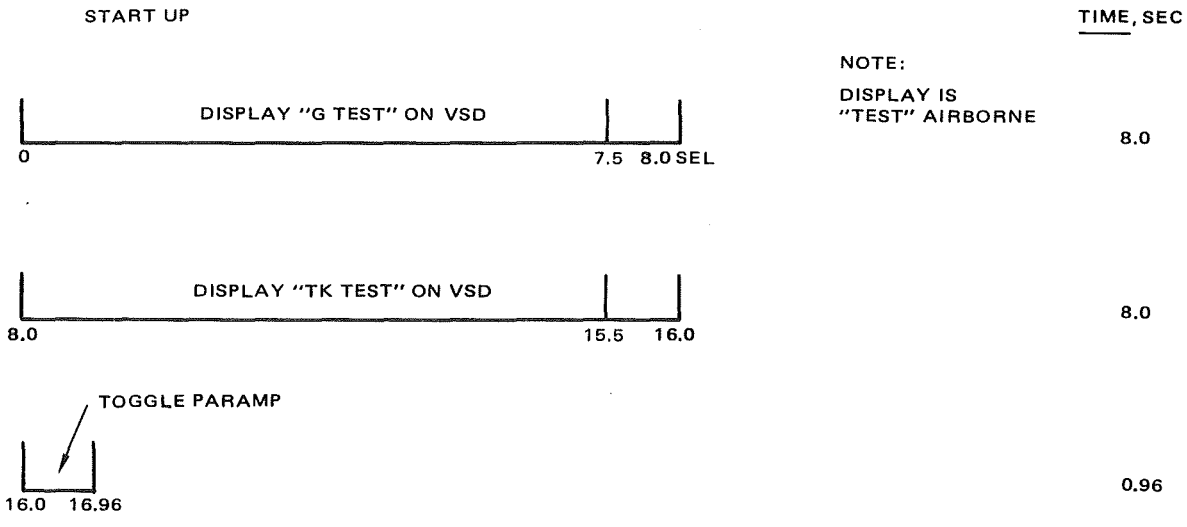

Figure 4.1-1. Operate initiated BIT time line. (Sheet 1 of 10)

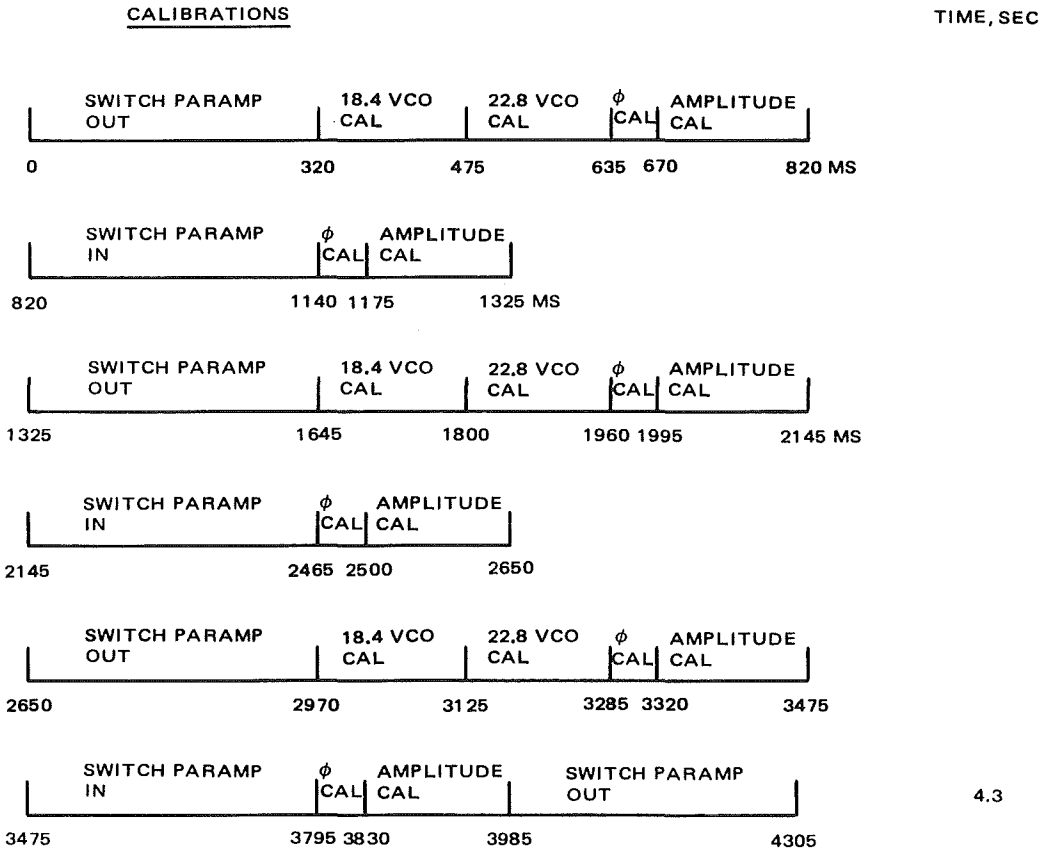

Figure 4.1-1. Operate initiated BIT time line. (Sheet 2 of 10)

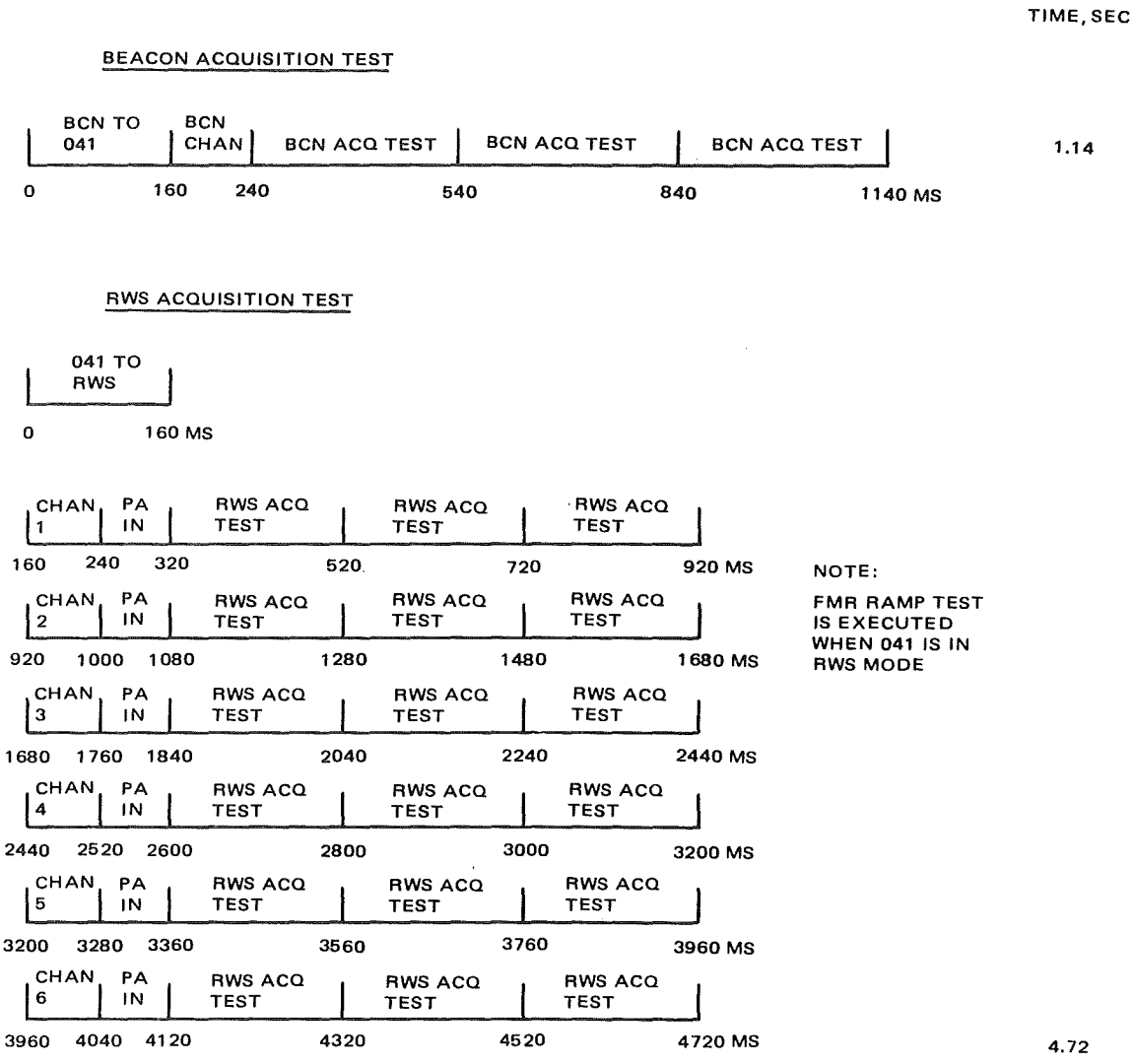

Figure 4.1-1. Operate initiated BIT time line. (Sheet 3 of 10)

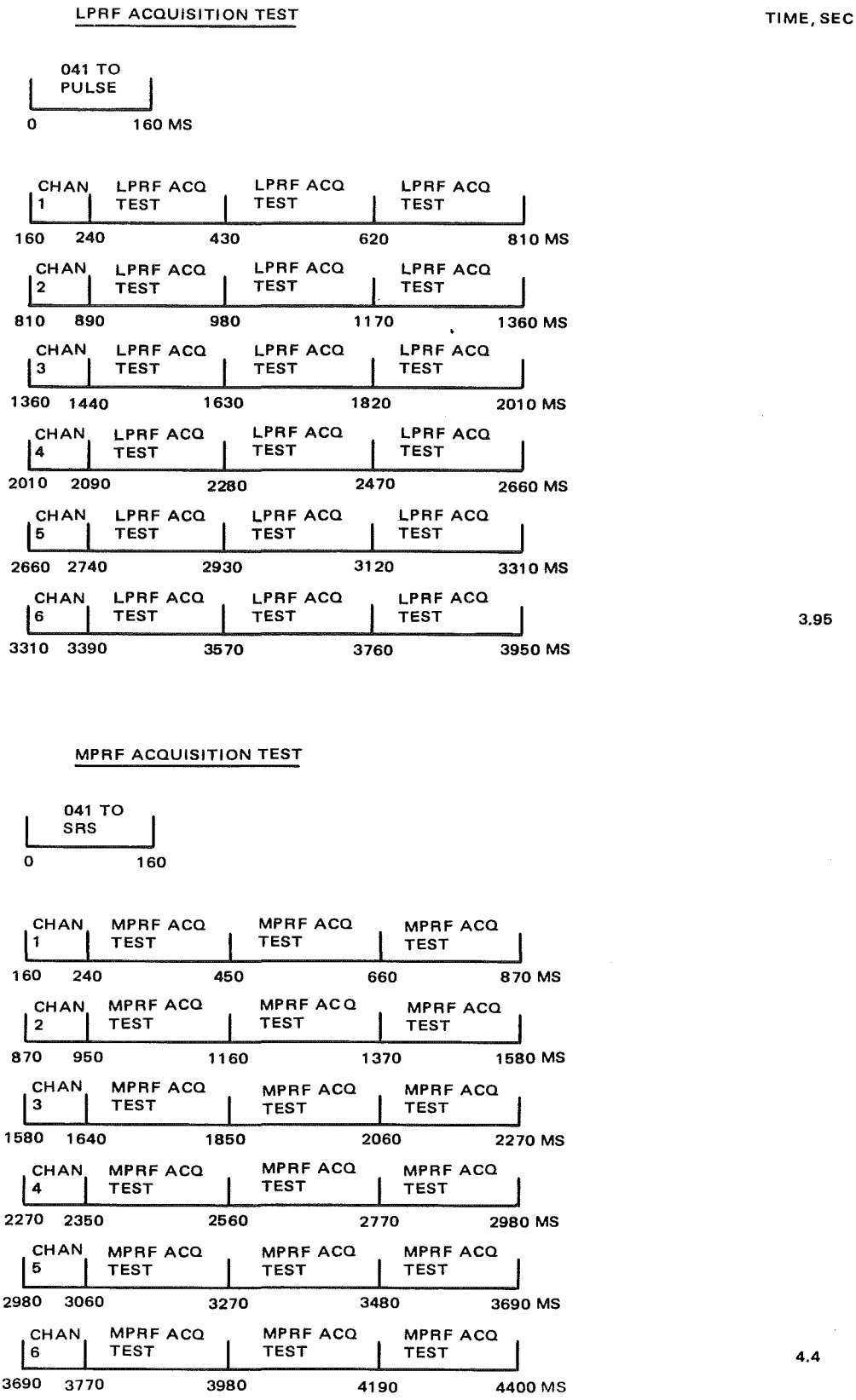

Figure 4.1-1. Operate initiated BIT time line. (Sheet 4 of 10)

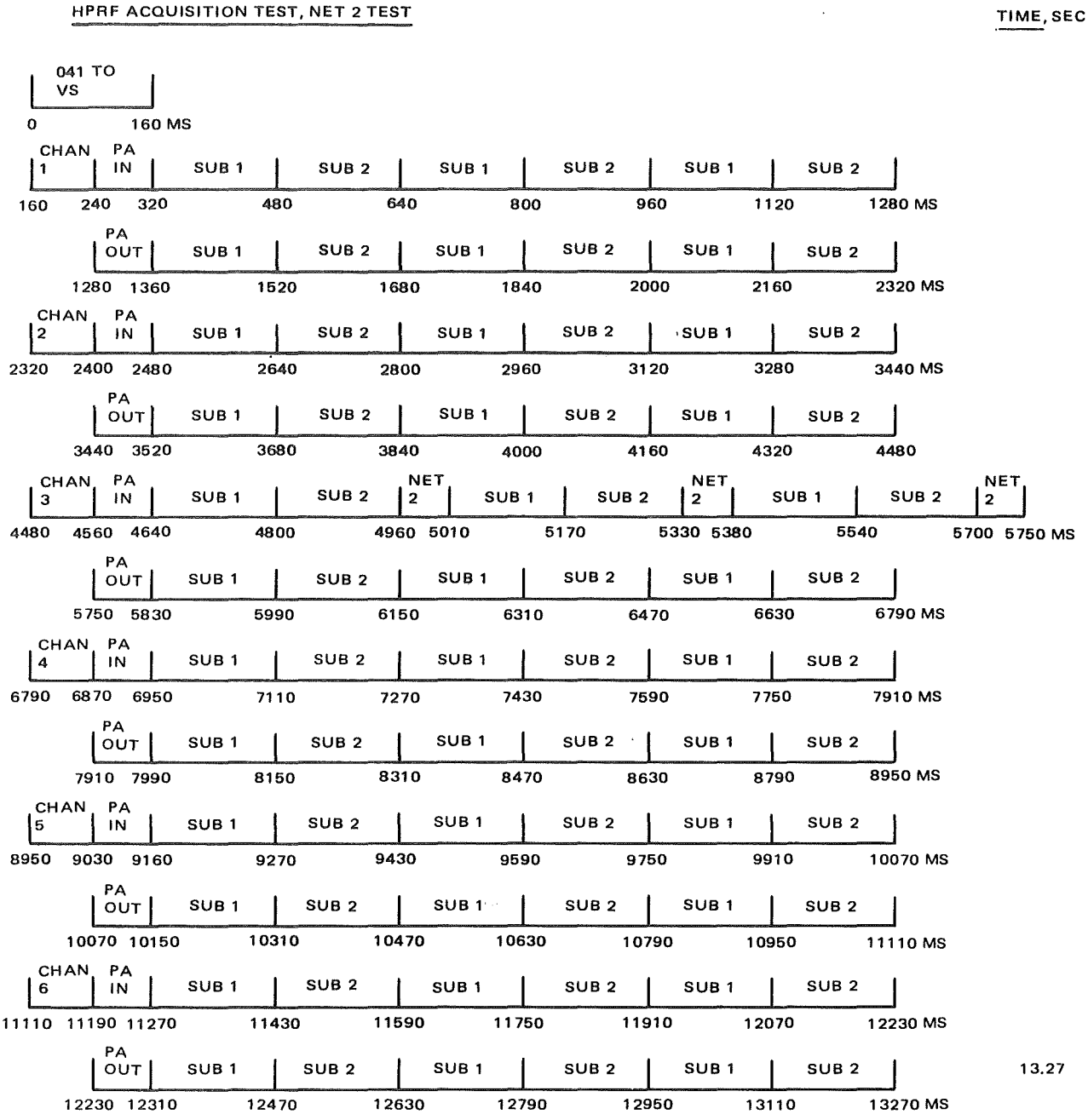

Figure 4.1-1. Operate initiated BIT time line. (Sheet 5 of 10)

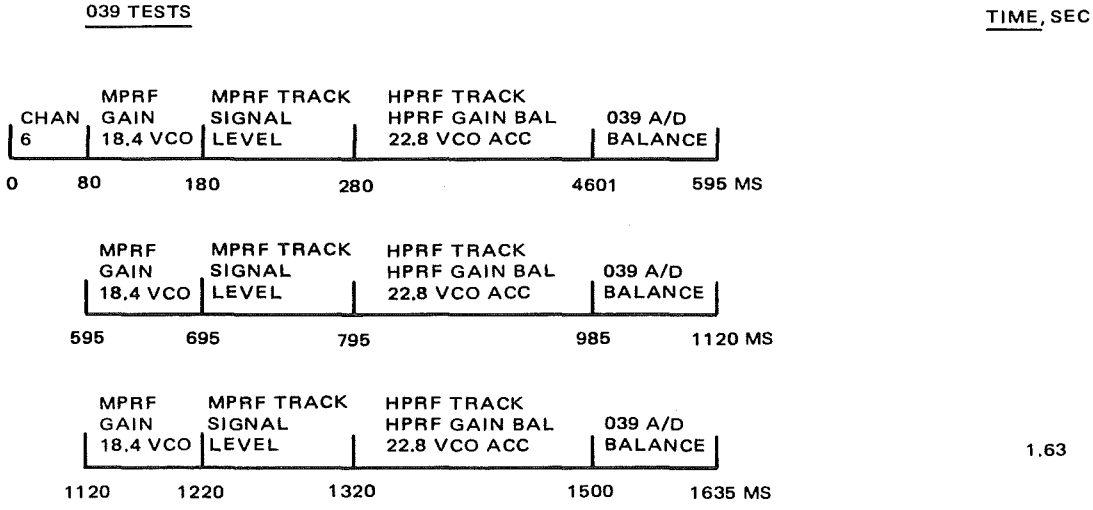

Figure 4.1-1. Operate initiated BIT time line. (Sheet 6 of 10)

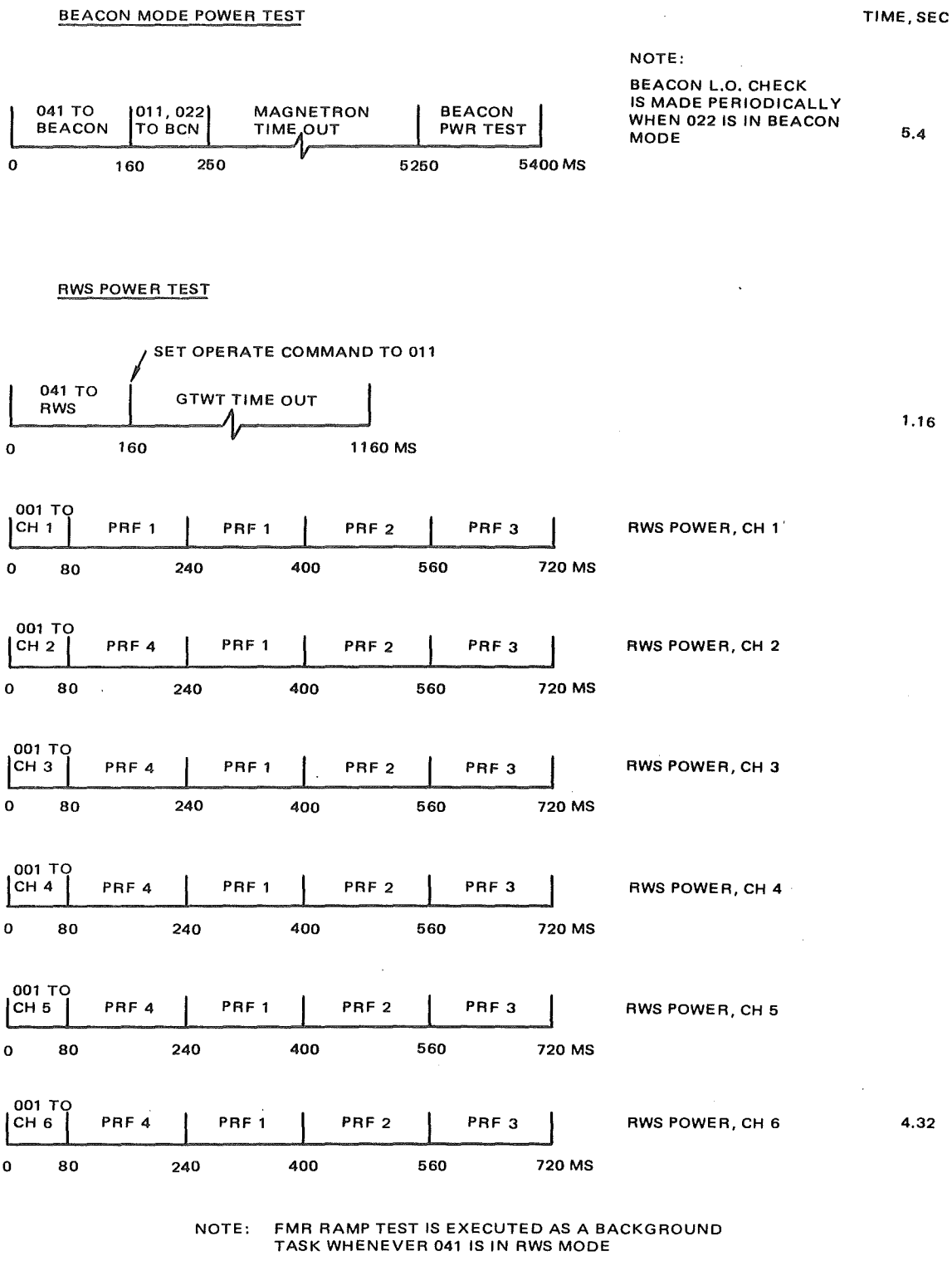

Figure 4.1-1. Operate initiated BIT time line. (Sheet 7 of 10)

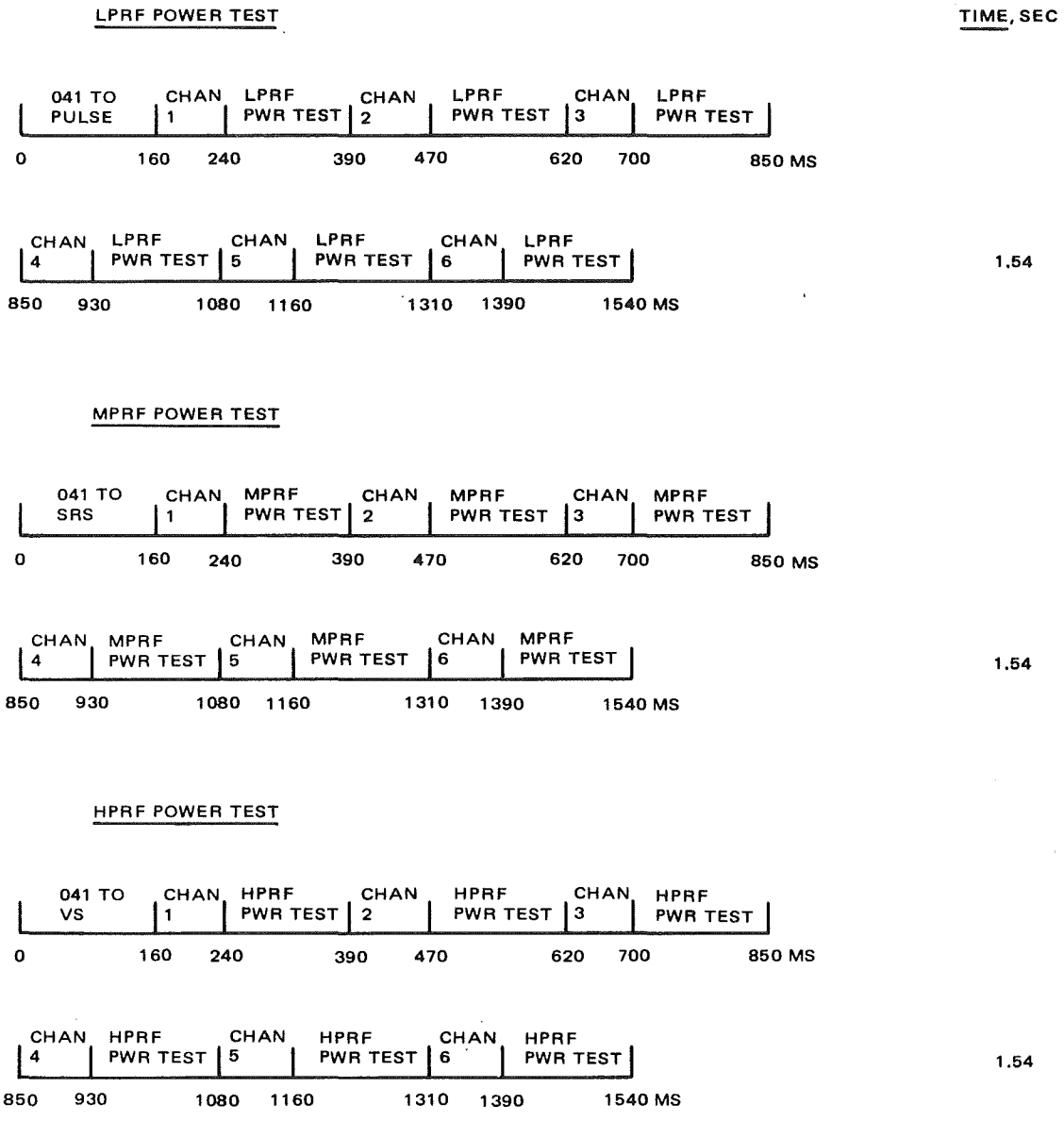

Figure 4.1-1. Operate initiated BIT time line. (Sheet 8 of 10)

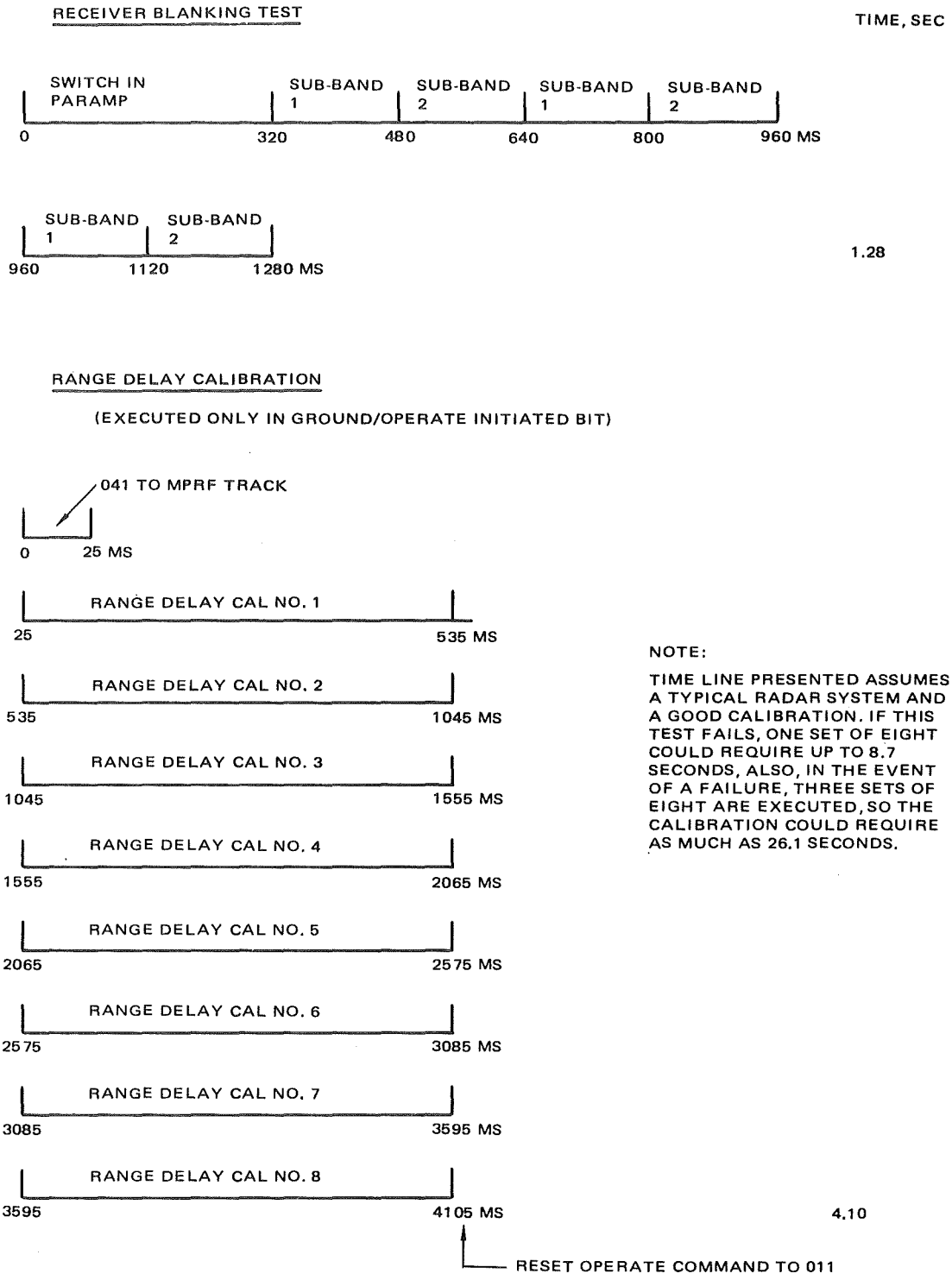

Figure 4.1-1. Operate initiated BIT time line. (Sheet 9 of 10)

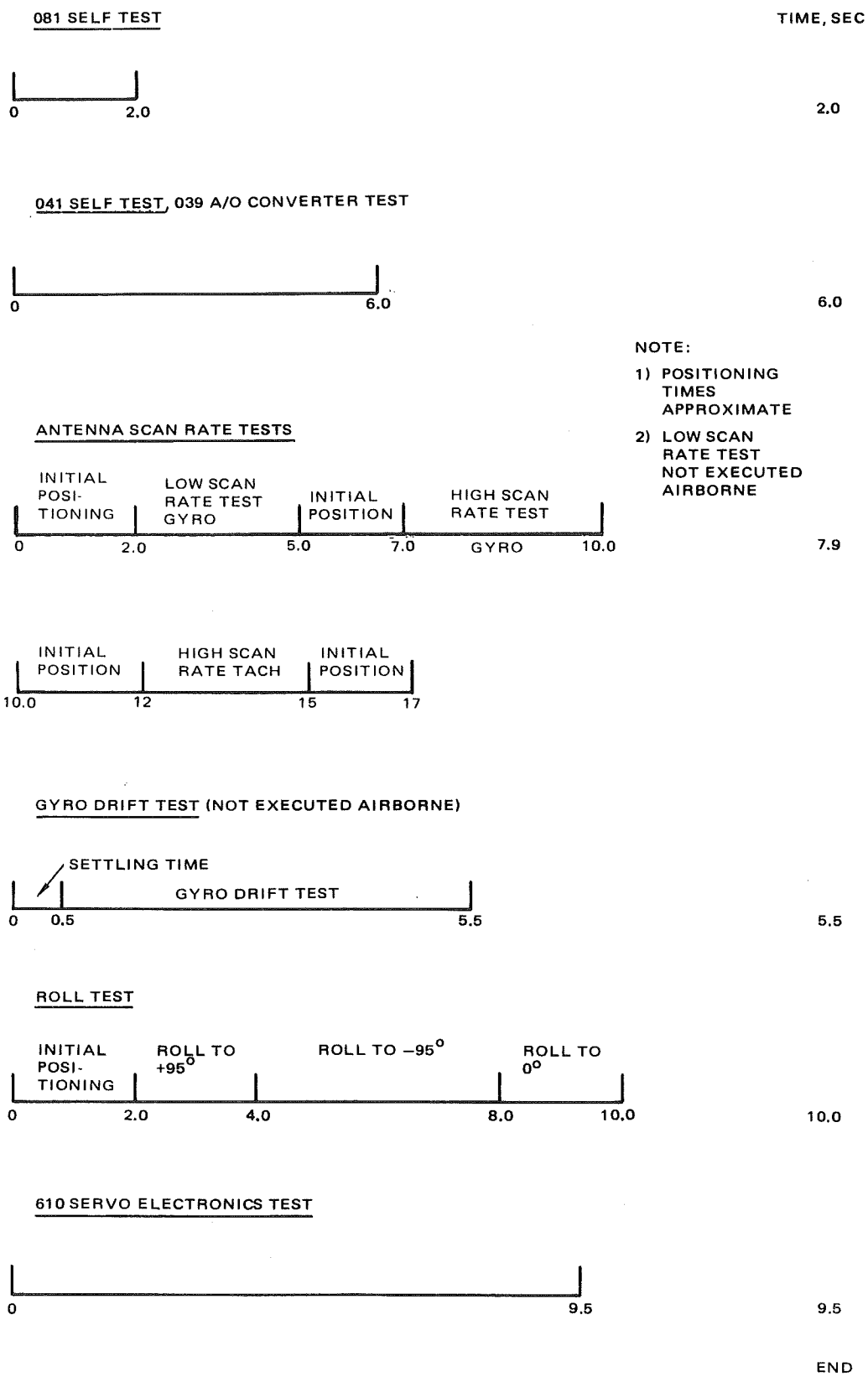

Figure 4.1-1. Operate initiated BIT time line. (Sheet 10 of 10)

4.2 CONTINUOUS MONITOR TIMING

The timing of the continuous monitor BIT tests is more complicated than Initiated BIT timing. This is because in Initiated BIT mode, the BIT software has control of the radar system, and can schedule events without serious interruption. In continuous monitor mode the tactical software has control of the task scheduling, and BIT tasks must be interleaved with the higher priority tactical tasks. The combination of the fact that BIT tasks must be time-shared with tactical tasks, and that the BIT tasks have lower priority make the continuous monitor BIT timing very erratic. It is so erratic that it is impossible to predict precisely when the tests will occur.

The description of continuous monitor BIT timing is divided into four parts — power up, shutdown, mode entry, and in mode. In each of these four cases, failures are recorded in the continuous monitor matrix.

4.2.1 Power Up BIT Tests

Power up is defined as beginning when the operator moves the power switch from the "OFF" position, and ending with the radar set enters the selected mode. The timing of the BIT tests occurring during this period is the subject of this section.

It should be noted that the power up sequence of BIT tests is also executed after long power transients. A long power transient is defined as a power transient of sufficient duration that the transmitter time out signal (from the 011 to the 081) goes to the reset state. For most radar systems this usually means a power loss of from 1 to 10 seconds. Power losses for more than 10 seconds are almost certainly long transients, while power losses for less than 1 second are almost certainly short transients. Between 1 and 10 seconds the transient may be long or short, depending on the particular unit.

The first milestone in the radar turn-on sequence is reached when:

1. A satisfactory coolant flow rate to the transmitter has been established
2. Five minutes has elapsed since turn-on.

Under normal circumstances, condition one will be satisfied within 5 seconds of turn-on. If condition two must be used to reach the first milestone, a coolant fault is set in the continuous monitor BIT matrix, and NoGo is sent to the BIT Control Panel.

The second milestone in the radar turn-on sequence is reached when, two and one-half minutes has elapsed since turn-on. The second milestone triggers the following BIT activity:

1. 081 Self Test
2. Fault Annunciator Test
3. 041 Self Test
4. Set annunciators on faulty units.

It should be noted that these milestones must be reached in order, i.e., the second milestone cannot be reached before the first milestone is reached. Thus, if it took five minutes to reach the first milestone, the second milestone would have been reached simultaneously.

The third milestone in the turn-on sequence is reached when:

1. Transmitter time-out is sent from the 011 to the 081
2. Three and one-half minutes has elapsed since the first milestone was reached.

The normal circumstance is that condition 1 satisfies milestone 3. If transmitter time-out is not sent, and condition 2 satisfies milestone 3, a transmitter time-out fault, and a 011 fault is set in the Continuous Monitor BIT matrix, and NoGo is sent to the BIT Control Panel.

Once the third milestone is reached the turn-on sequence is over. The system then starts mode entry proceedings.

The longest startup sequence will result when no coolant flow is established. This takes eight and one-half minutes. If the radar set has not entered the selected mode in eight and one-half minutes, it probably will not come up.

Simultaneous with the activity described above, BIT executes the following tests:

1. Checks for 610 operational every 50 milliseconds. If the 610 ever indicates non-operational status, an attempt is made to

restart the 610. Three unsuccessful restarts over a 16 second period will result in a 610 power fault in the Continuous Monitor BIT matrix, and a NoGo to the BIT Control Panel. More importantly, the radar will shut down.

2. Exciter lock tests and L.O. power (every two seconds).
3. Radar overheat (continuously).
4. Energizer fault (every process sync).
5. Check sum on the fly.
6. Watchdog Interrupt.
7. Process Sync and IDA Interrupt.

4.2.2 Shutdown BIT Tests

Like power-up, shutdown is a period of low BIT activity. The primary BIT function at shutdown is not system testing, but testing and setting fault annunciators.

When the power switch is turned to the "OFF" position, BIT executes the limited fault isolation procedure described in Section 2.1. Fault annunciators are tested then set on any units that are tagged faulty in either the Initiated BIT matrix, or the continuous monitor matrix. After setting the fault annunciators, BIT relaxes and looks forward to a rest.

The shutdown sequence takes less than one second. BIT activities are completed in the first few microseconds of the shutdown sequence.

4.2.3 Mode Entry BIT Tests

At mode entry, system calibrations are executed. The calibrations executed are:

1. 18.4 MHz VCO calibration (154.8 ms)
2. 22.8 MHz VCO calibration (161.3 ms)
3. Receiver Phase Calibration (34.4 ms)
4. Amplitude Calibration (151.5 ms).

in that order.

These calibrations are not executed at this time to test the system, but to calibrate it. They are included as a part of BIT because they have the capability of setting the NoGo light and setting faults in the BIT matrix.

The mode entry calibrations require in excess of one-half second to execute. Thus, these calibrations are executed only on entry to modes when loss of one-half second is not deemed critical. For example, the mode entry calibrations are executed at entry to Search modes, where loss of one-half second before searching begins is not critical; mode entry calibrations are not executed on entry to Acquisition II, as loss of one-half second then might mean missing the target configuration.

Basically, mode entry calibrations are executed at all mode changes, except the following:

1. Transition from Acquisition I to Acquisition II
2. Transition from Acquisition II to Track
3. Entry to Beacon mode
4. Entry to Velocity Update mode
5. During turn on of the radar set
6. Under some ECCM conditions.

This leaves entry to Search modes, entry to Acquisition I modes, and entry to Reacquisition modes as the primary times when mode entry calibrations are executed.

4.2.4 In Mode BIT Tests

The In Mode BIT tests are commonly referred to as the Continuous Monitor tests. The philosophy behind these tests is to make periodic checks of radar performance while the system is in tactical operating mode. Included in these checks are periodic system calibrations.

The types of periodic tests executed fall into three categories:

1. System Monitor tests
2. System Sensitivity and 039 tests
3. System Calibration.

The System Monitor tests are those tests where the system provides BIT data to the 081 without any active test initiation by the BIT software. These are:

1. Process Sync and IDA Interrupt tests (continuously)
2. Check Sum test (continuously)

3. Radar Overheat test (continuously)
4. Watchdog Interrupt test (continuously)
5. GTWT Drive Lock, Offset Lock, L.O. Power (executed at two-second intervals in modes where the 001 unit provides the L.O. and GTWT drive signals)
6. FMR Ramp (executed continuously when the 041 is in RWS mode)
7. RF Power tests (executed at two-second intervals whenever Beacon command is sent to the 011)
8. Transmitter Time Out, Coolant/Waveguide Pressure, Multipactor, Dummy Load (executed at two-second intervals)
9. Az/El Diode (executed every process sync period)
10. AIP (executed at Scan initialization in Scan modes, and continuously in Antenna Positioning modes)
11. Roll and Scan Rate (executed continuously during antenna scanning modes)
12. Energizer (executed every Process Sync period)
13. Beacon L.O. (every two seconds when the 022 is in Beacon Mode).

The system sensitivity tests and 039 tests are executed only in Antenna Scan Search modes. These tests are executed at end of bar periods which are also end of frame periods. The tests are executed at a minimum spacing of six seconds.

In general the MPRF Track Signal Level, MPRF Gain Balance, and 18.4 MHz VCO Frequency Accuracy tests are executed in all antenna scan modes. In addition within each mode, some sensitivity tests peculiar to that mode are executed. They are:

- VS
  - VS Sub-Band 1
  - VS Sub-Band 2
  - HPRF Track
  - HPRF Gain Balance
  - 22.8 MHz VCO Frequency Accuracy
- LRS
  - RWS Acquisition
  - MPRF Acquisition

- SRS
  - MPRF Acquisition
- Beacon
  - Beacon Acquisition
- All LPRF
  - LPRF Acquisition.

The timing of the tests is controlled by a six second timer in the BIT software. At end of frame, the timer is checked to see if six seconds has elapsed. If it has, the first of the tests for that mode is executed, and a new six second timer is started. At the next end of frame, another test is executed until all tests to be executed for that mode are completed. At this point the six second timer is checked to see if it has expired. If not, no tests are executed at end of frame until six seconds has expired. If and when the timer expires, a new series of tests is started. In most cases the timer expires before the test series is completed, so that there are no end of frames skipped.

The final category of periodic tests is System Calibration. In HPRF and MPRF Antenna Scan Search modes, the 18.4 MHz and 22.8 MHz VCOs are calibrated at end of bar periods which are not end of frame periods. The same six second scheme is used. At each end of bar the timer is checked. When the timer expires, a new timer is started and the 18.4 MHz VCO calibration is executed. At the next end of bar the 22.8 MHz VCO calibration is executed. Then wait for the six second timer to expire. The periodic calibrations are inhibited under some ECCM conditions.

System calibrations are also periodically executed in track mode. In HPRF track the sequence is:

1. 18.4 MHz VCO calibration
2. 22.8 MHz VCO calibration
3. Phase and Amplitude calibration (executed at three second intervals.

In LPRF and MPRF track the two VCO calibrations are executed together followed by a six second wait. The Phase and Amplitude calibrations are then executed followed by a three second wait; the sequence then repeats with the VCO calibrations.

System calibrations in Track can be inhibited subject to signal to noise, angle tracking, and ECCM considerations.

5.0 BIT TARGET GENERATION AND CONTROL

5.1 GENERAL DESCRIPTION

RF signal detection and processing capabilities of the radar set are verified by the system response to target signals generated by Built-In Test (BIT). These RF target signals are generated at the X-band pulse doppler (PD) carrier frequency. They are classified according to their method of generation and utilization as BIT antenna targets, BIT receiver targets, and BIT precision range targets. The BIT target signals are generated and coupled into the radar set as shown in the block diagram, Figure 5.1. Table 5.1 summarizes the signal characteristics of each target signal. A complete description of each BIT signal is presented in the following paragraphs.

5.2 BIT ANTENNA TARGET

The BIT antenna target provides test signals for Built-In-Test, for receiver phase and gain calibrations, and for calibrating the voltage controlled oscillators (VCOs) in the analog radar signal processor (ARSP).

The BIT antenna target provides two signals to the radar set — one at the sum output port and one at the guard/difference output port of the antenna. These signals have a relative phase shift that differs by 90 degrees from that which would be generated by a target located at the antenna sum/difference pattern crossover (down and to the left of boresight).

The target signal is designed to provide a signal to the receiver sum (Σ) channel input of -60 dBm ± 5 dB and a signal to the receiver guard/difference (G/Δ) channel input that differs by less than 5 dB from that at the Σ channel input. The target signal levels and signal paths are illustrated in Figure 5.2.

[This is technically page #160. The diagram on page 161 considers the back to be page 162, so while it appears otherwise, there are no missing pages. Page 161 is a fold-out diagram.]

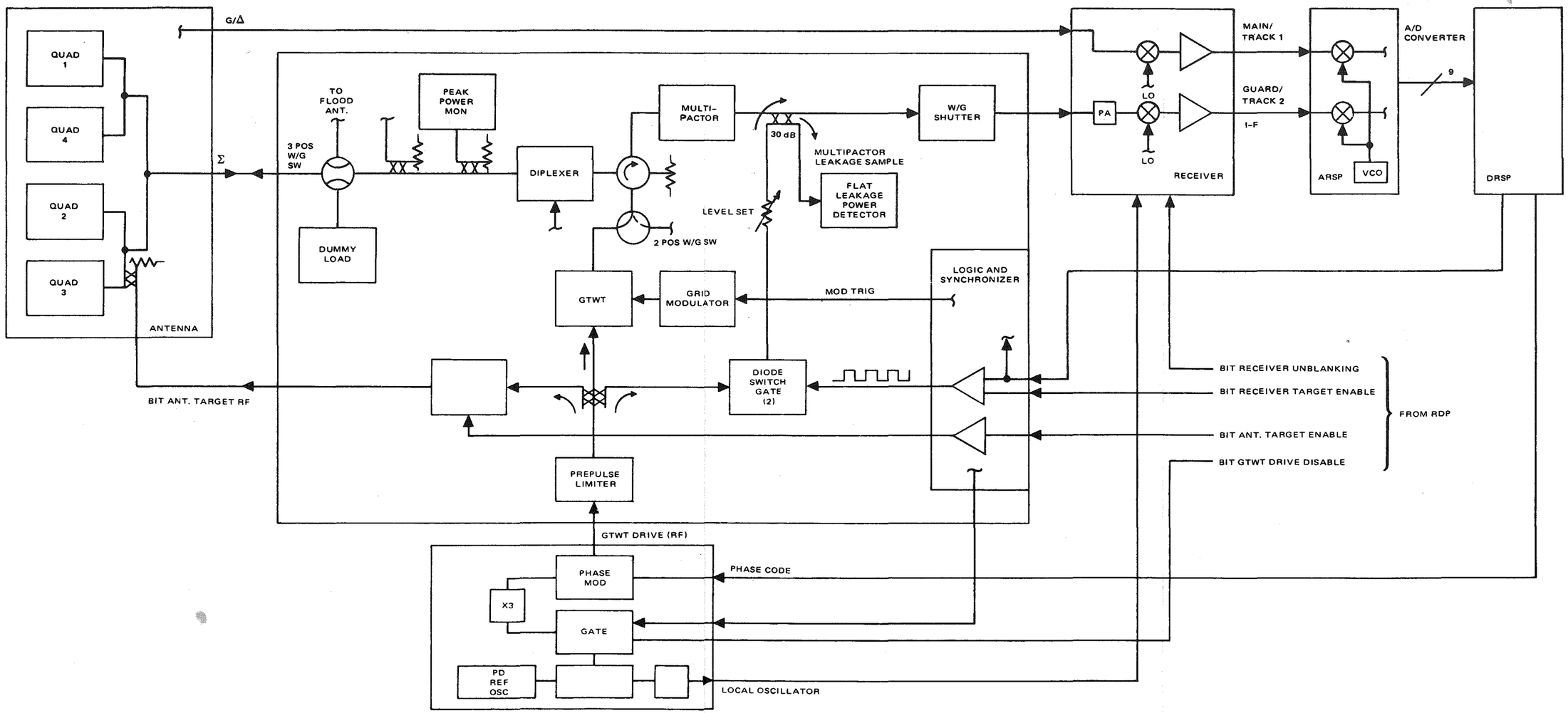

Figure 5.1. BIT RF Target Generation Block Diagram

TABLE 5.1 BIT TARGET SIGNAL CHARACTERISTICS

BIT Target	Rcvr Channel Used	PRF	Target Signal	Pulse Width	Doppler Shift	Pulse Delay	Signal Power (Rcvr Input)	Pulse Timing Source
BIT Antenna Target	Σ and G/Δ	HPRF	CW RF	-	0 kHz	-	-60 dBm ±5 dB	None
		MPRF	Pulsed RF	1 or 13 range bins	0 kHz	Note 1	(-60 dBm ±5 dB) x df Note 3	DRSP-BIT MPRF range delay gen.
		LPRF	Pulsed RF Train	1 to 13 μs	0 kHz	Note 2	Same as above	DRSP-BIT LPRF range delay gen.
BIT Receiver Target	Σ	HPRF	Pulsed RF Spectral Lines	67 μsec	±n x 7.44 kHz for n = 1, 3, 5..	-	-85 dBm ±1.7 dB peak See Figure 5.3.1	DRSP - square wave source
BIT Precision Ranging Target	Σ	MPRF	Pulsed RF	20.8 μsec	0 kHz	20 range bins	-38 dBm peak	DRSP-BIT MPRF range delay gen.

NOTES:
1. Pulse delay in MPRF varies according to the selected PRF to provide targets at 7.0, 9.1, or 11.1 n.mi. range.
2. Pulses are spaced every 65 μsec (5.24 n.mi.).
3. Duty factor (df) varies according to the selected PRF.

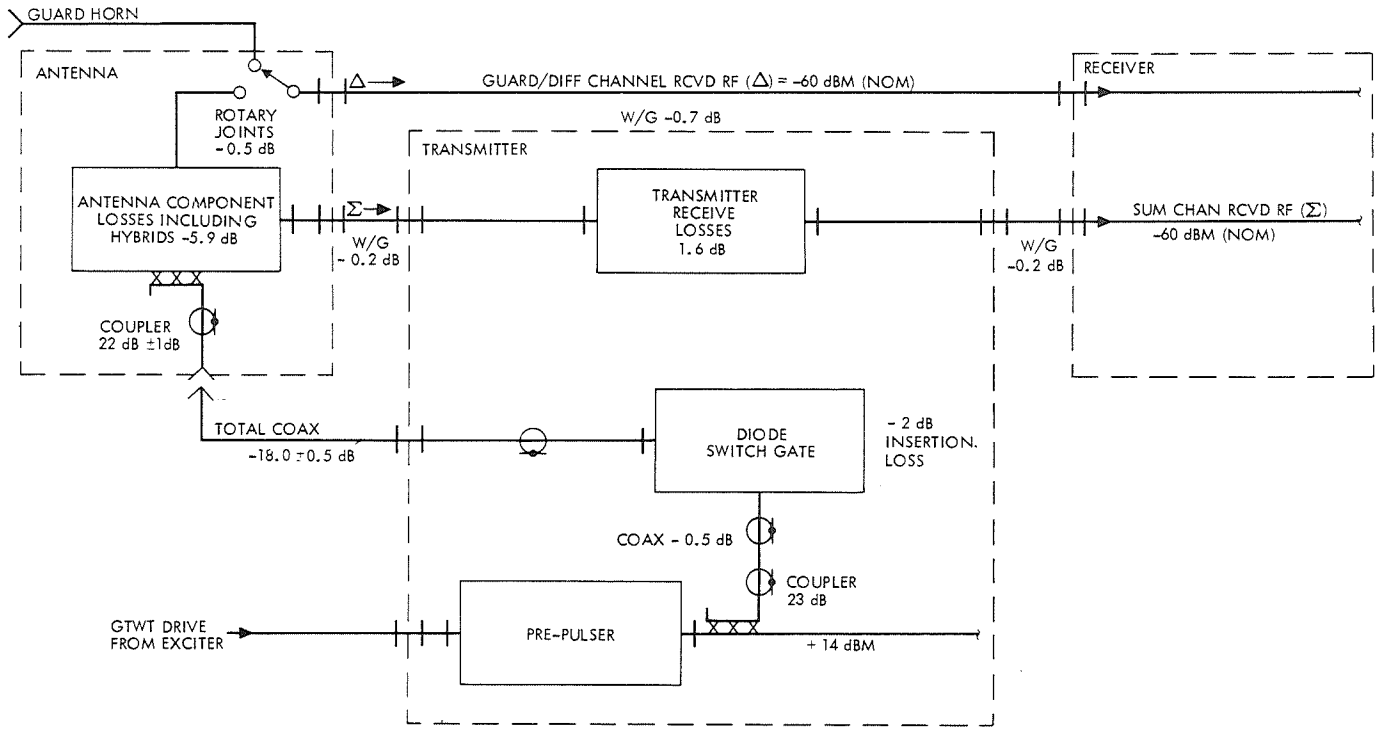

Figure 5.2. BIT Antenna Target Losses

The BIT antenna target is enabled by the discrete BIT antenna target enable signal from the RDP to the transmitter. This signal enables the PIN diode gate (1) shown in Figure 5.1 to couple a specific amount of GTWT drive signal into the 3rd quadrant of the antenna hybrid structure.[1] This signal is routed through the antenna structure to the sum and guard/difference output ports.

The relative phase angle between the two target signals is determined by the antenna hybrid structure and the entrance point of the target signal from the transmitter. The Δ channel output signal leads the Σ signal by $\theta + 90$ degrees, where θ is an arbitrary phase angle that exists between the Σ and Δ output ports during track of a target which is down or to the left of antenna boresight.

Modulation of the BIT antenna target signal is determined by the form of the GTWT drive gate signal to the exciter from the transmitter. This signal is dependent upon the mode of operation of the transmitter. It gates the GTWT drive signal to form pulsed RF signals in the L/M PRF modes or to generate unmodulated (CW) RF energy in the HPRF mode. In the pulse compression L/M PRF modes, the pulsed signals are also phase coded by the phase code signal from the DRSP unit.

Target range is simulated in the L/M PRF modes by delaying the generation of the pulse modulation with respect to the master timing clock. This is accomplished in the DRSP by delaying the L/M PRF pulses and phase code signals. In the MPRF mode, the resultant range of the BIT target is 7.0, 9.1, or 11.1 NMi, depending on the selected major MPRF. In the LPRF mode, targets are generated every 5.24 NMi.

The BIT antenna target signals are generated at the selected PD carrier frequency, that is, they represent target signals with zero doppler frequency shift. If it is required to generate a target having a given doppler frequency shift in the search mode, the target signal is mixed with the main

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[1] Note: This energy is also transmitted out the antenna 3rd quadrant array and may reflect back into the guard antenna if in close proximity to a reflective barrier such as a building or runway apron.

with the VCO calibrations, lobe clutter (MLC) VCO in the ARSP as shown in Figure 5.1, to produce a down-converted target signal of the desired frequency shift.

The basic radar set configuration required to process the BIT antenna target is as follows:

1. The BIT Antenna Target is enabled
2. The GTWT is disabled by the SNIFF command
3. The radar planar array antenna is selected
4. The receiver is unblanked
5. The antenna channel selector switch is set to the guard channel in acquisition testing and difference channel in track testing
6. The DRSP is commanded to CM BIT mode.

Item 2 above is selected by commanding the transmitter to the SNIFF mode. Item 4 is accomplished by the BIT receiver unblanking signal from the RDP. The remaining items are set by mode logic and/or BIT commands as required.

5.3 BIT RECEIVER RF TARGET

The BIT receiver RF target is generated in the HPRF search mode and RWS search mode to measure the detection sensitivity of the radar set and in track tests. The target signal consists of a series of spectral lines above and below the central line (the PD carrier) frequency. The spectral lines represent doppler shift target signals of known frequencies and signal strengths. The spectrum is illustrated in Figure 5.3.1-1.

The target signal is enabled by receipt of the discrete BIT receiver target enable signal from the RDP. As shown in Figure 5.1, this command enables the PIN diode gate (2) allowing the gate to square-wave modulate the GTWT drive signal sample. The resulting signal is coupled to the receiver sum channel input.

The square wave modulation signal is obtained from the digital radar signal processor (DRSP) and is sent to the transmitter on the L/M PRF line. Its frequency, 7.44 KHz, determines the spacing of the RF spectral lines.

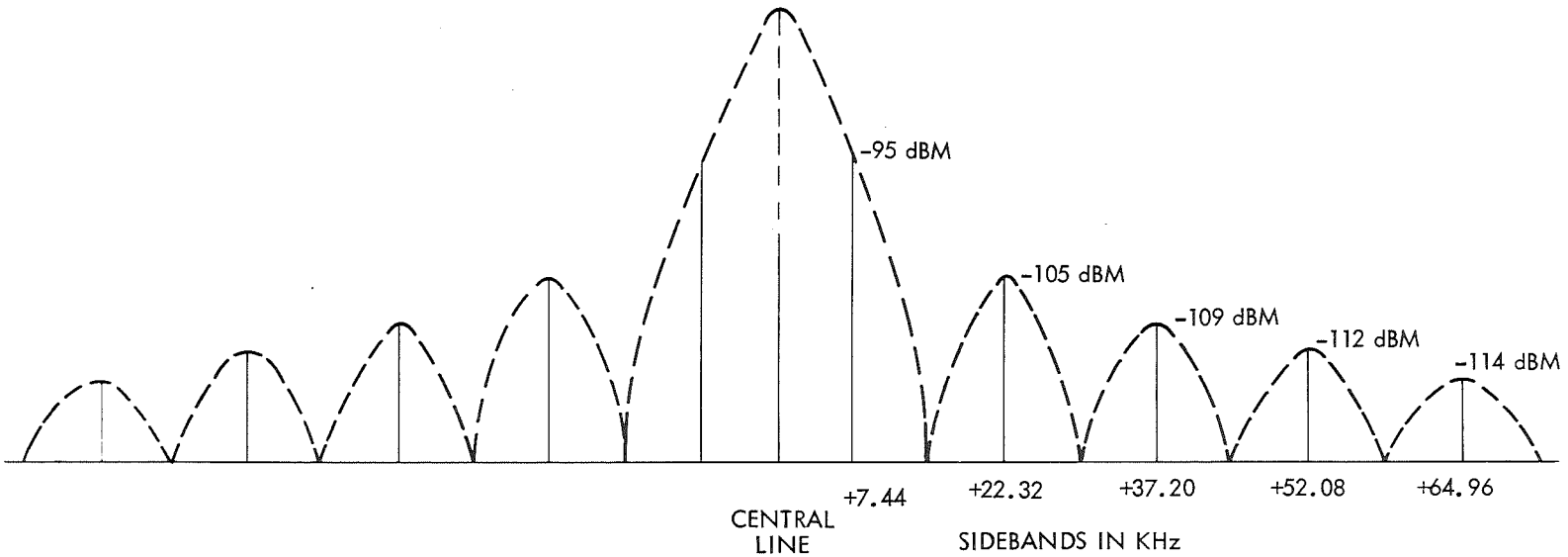

Figure 5.3.1-1. HPRF target spectrum.

The square-wave determines the relative magnitudes of the spectral lines. The peak power of the BIT target is adjusted by the transmitter level set adjustment shown in Figure 5.1 to -85 dBm at the receiver sum channel input port. The resulting power in each spectral line is shown in Figure 5.3.1-1.

The BIT receiver target RF signal path and RF losses are shown in Figure 5.3.2-1.

The following radar set configuration must be selected to insure the presence of the target signal at the receiver sum channel input:

1. The BIT Receiver Target is enabled
2. The GTWT is disabled by commanding SNIFF
3. The Receiver is unblanked
4. The DRSP is commanded to CM BIT mode.

Item 2 is selected by commanding the transmitter to the SNIFF mode. The receiver is unblanked by the BIT receiver unblanking command from the radar data processor (RDP).

5.4 BIT PRECISION RANGE TARGET

The BIT precision range target provides a replica of the RF output pulse of the GTWT. It is used to measure the fixed system delays of the radar set.

The BIT precision range target signal is generated in the medium PRF mode, a 1.6 μsec short pulse width is selected, the GTWT is in operation, and the GTWT drive signal is enabled. The time delay between the centroid of the GTWT output pulse and the GTWT grid pulse forms the basis of the range delay calibration.

The RF pulse from the GTWT output passes through the circulator and diplexer to the antenna as shown in Figure 5.1. The antenna reflects some of the incident energy back to the sum channel input of the transmitter. The signal passes through the transmitter to the receiver. The BIT precision range target RF pulse power at the receiver sum channel input is +17 dBm (nominal). (Limited by the limiter in the receiver.)

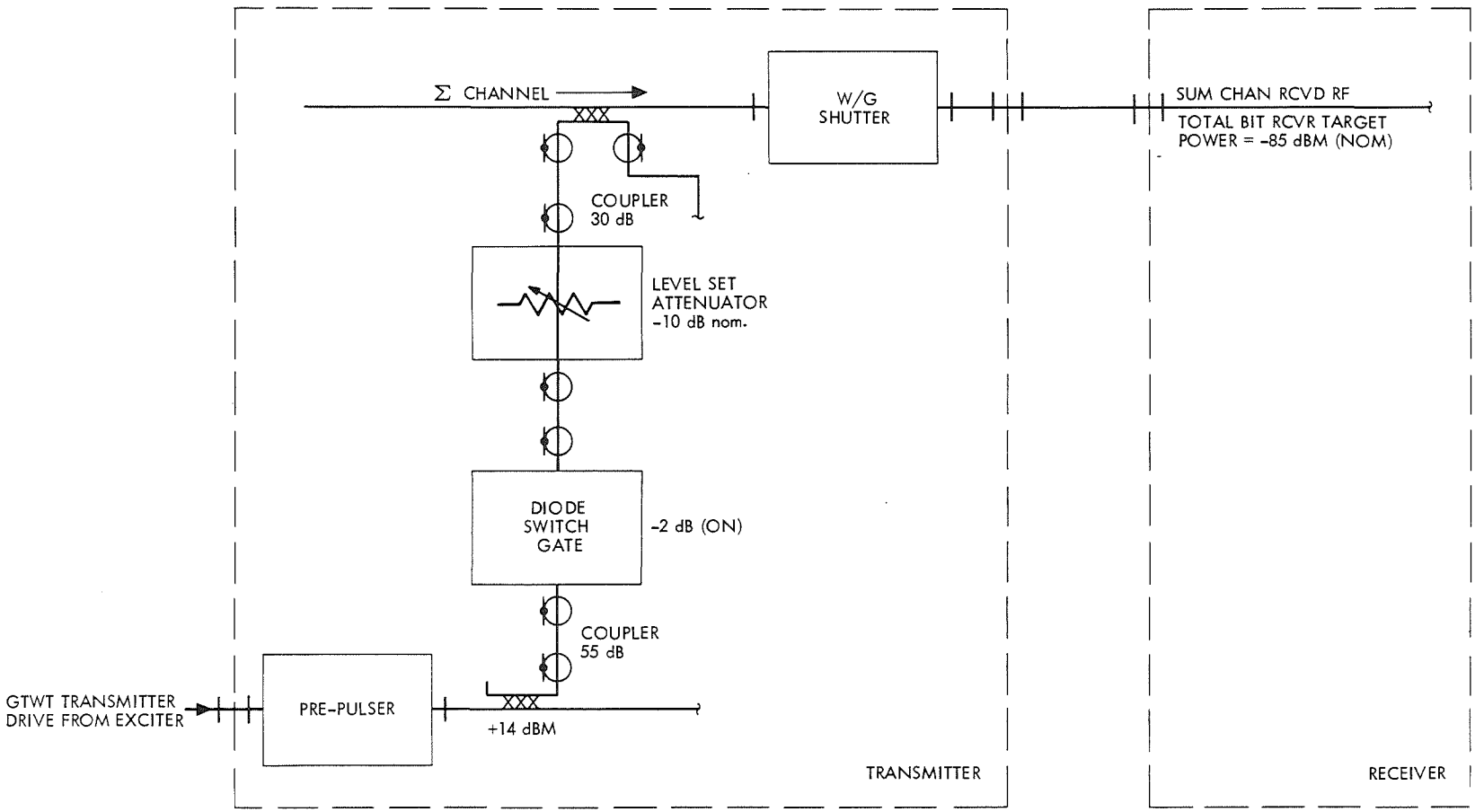

Figure 5.3.2-1. BIT receiver target losses.

The BIT precision range target is delayed in time with respect to the master timing clock to prevent it from being blanked at the A/D converter output of the analog radar signal processor (ARSP). The time delay is determined by the BIT MPRF range delay circuit in the DRSP which delays the MPRF pulses to the transmitter by a known amount.

The following radar set configuration must be selected to perform the range delay calibration:

1. The receiver is unblanked
2. MPRF SP Track is selected
3. RSP is commanded to MPRF Track.

6.0 SYSTEM BLOCK DIAGRAM

The attached block diagram contains the functional blocks required for the F-15 radar set.